

# MADVLSI Mini-Project 4

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## 1 Introduction

The goal of this project was to create a seven-bit current-output digital to analog converter using Xschem, Magic, and Skywater Technology's SKY130 PDK. The output current must be available as a current source or sink that changes by no more than 0.5%/V over at least 80% of the 1.8V power supply range. The circuit simulation results must show that without mismatch, the worst-case DNL is less than 2 LSBs and your INL is less than 4 LSBs and that, with mismatch, the worst-case INL and DNL are both less than 8 LSBs.

## 2 GitHub Repository

<https://github.com/kburp/current-output-dac-vlsi>

## 3 Design



Figure 1: Depiction of design process for MP4

## 4 Schematics

### 4.1 DAC

During the design process, we were presented with two primary DAC design options. The W-2W DAC and the design specified by Hammerschmied in 1998. Although the design specified by Hammerschmied has a significantly smaller INL and DNL than the W-2W without any peripheral devices, the inability to hold the  $I_{dump}$  and  $I_{sense}$  voltage potentials to a close level to maintain this INL and DNL when mirroring the output current meant that for these design specifications, the W-2W ladder was more suitable. Therefore, we chose to use the W-2W design for this project.

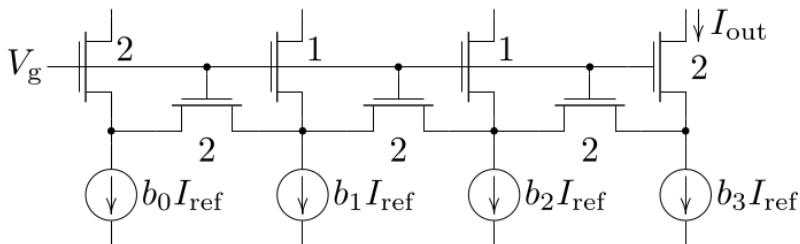


Figure 2: W-2W DAC Design

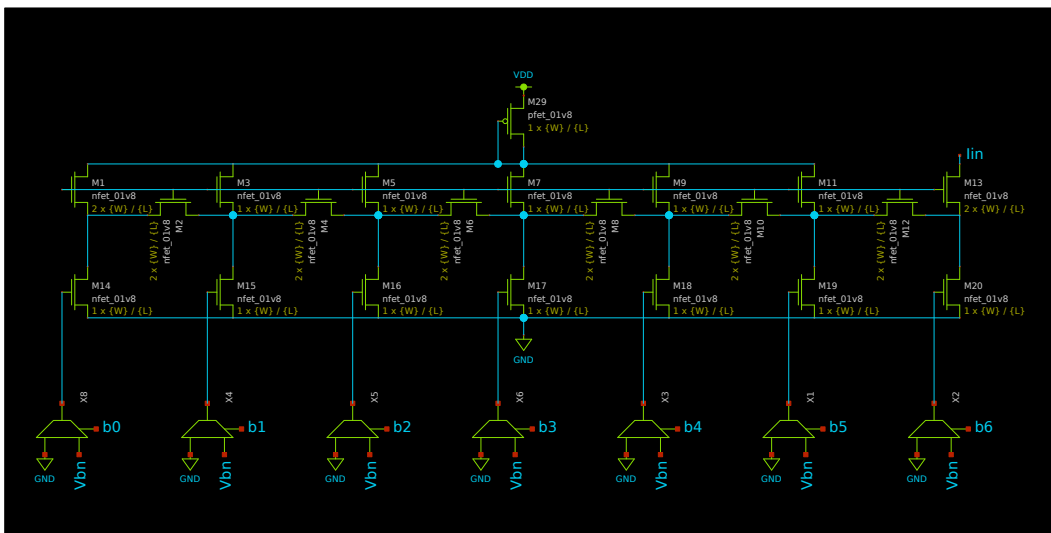


Figure 3: Schematic of DAC with Associated Input Multiplexers

#### 4.1.1 Transistor Sizing

After running Monte Carlo simulations with various transistor sizes, we found that the size that is best for most of the circuit is a width of 24 and a length of 1.

### 4.1.2 DAC Gate Voltage Generator

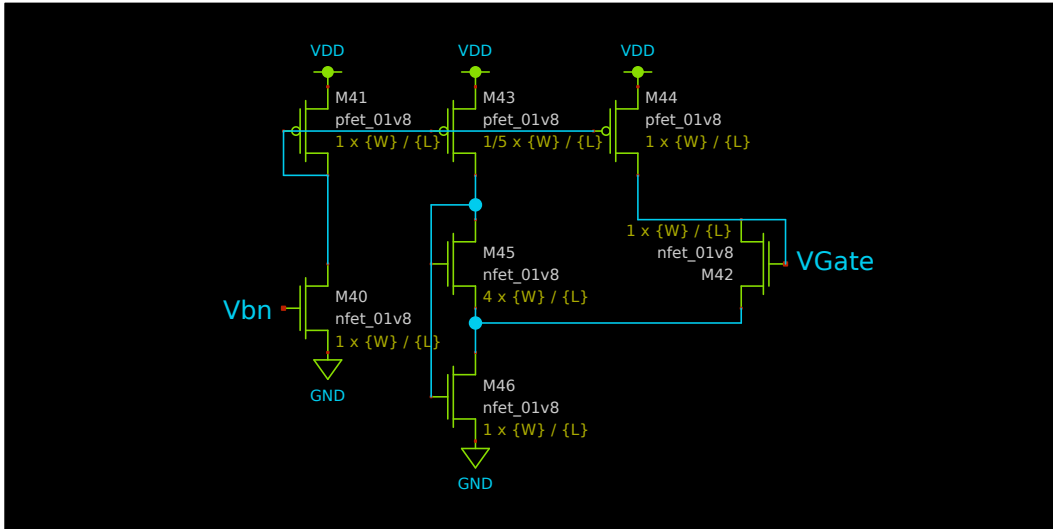


Figure 4: Design for the Gate Voltage Generator for the DAC

The gate voltage of the W-2W ladder network of the DAC was a cascode voltage created using a cascode bias voltage generator.

### 4.1.3 Multiplexers for Digital Inputs

Because the gate voltages of all of our input nMOS transistors when the bit is high needs to be Vbn, but our binary inputs are given at either VDD or GND, we use Multiplexers to switch between Vbn and GND based on the input.

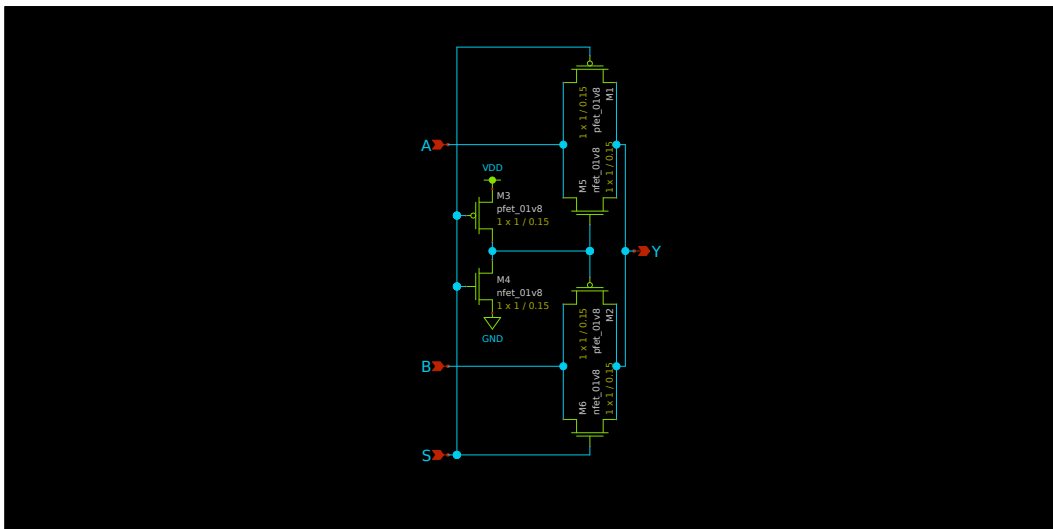


Figure 5: Schematic of MUX



# 5 Layout-Driven Schematic

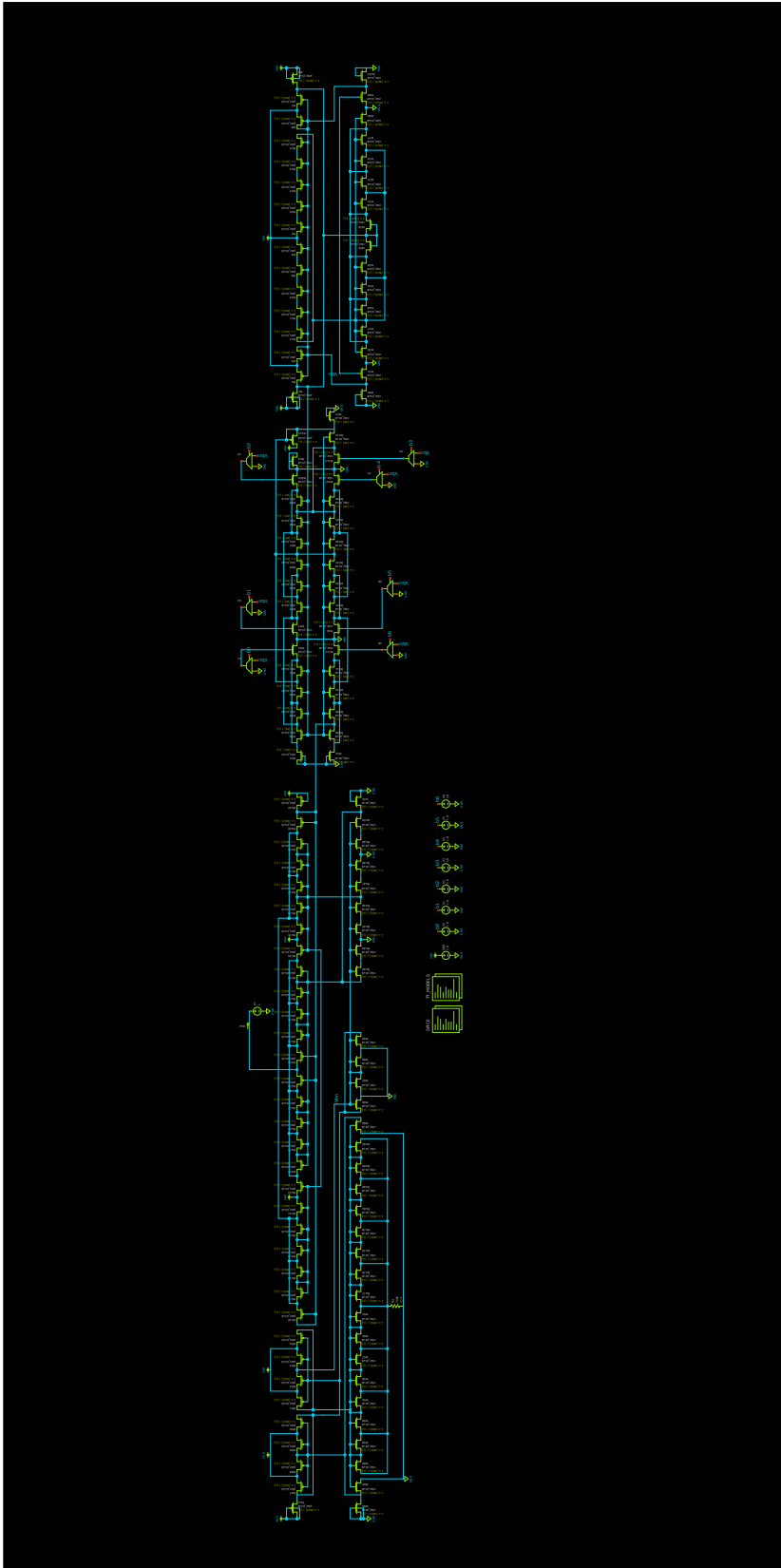


Figure 8: Layout-driven schematic of overall circuit.

In order to make our layout process easier, we created a layout-driven schematic of our overall DAC, including all of the peripheral components.

## 6 Testbenches and Simulations

All simulations were run on the layout-driven schematic.

### 6.1 DAC Transfer Characteristics

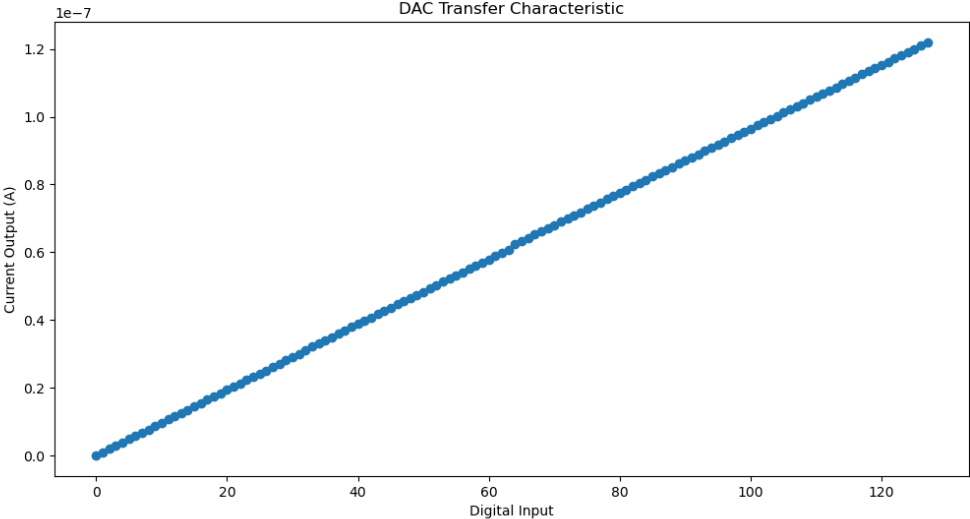


Figure 9: Digital input voltage to analog output current transfer characteristic of DAC.

## 6.2 Differential Non-linearity

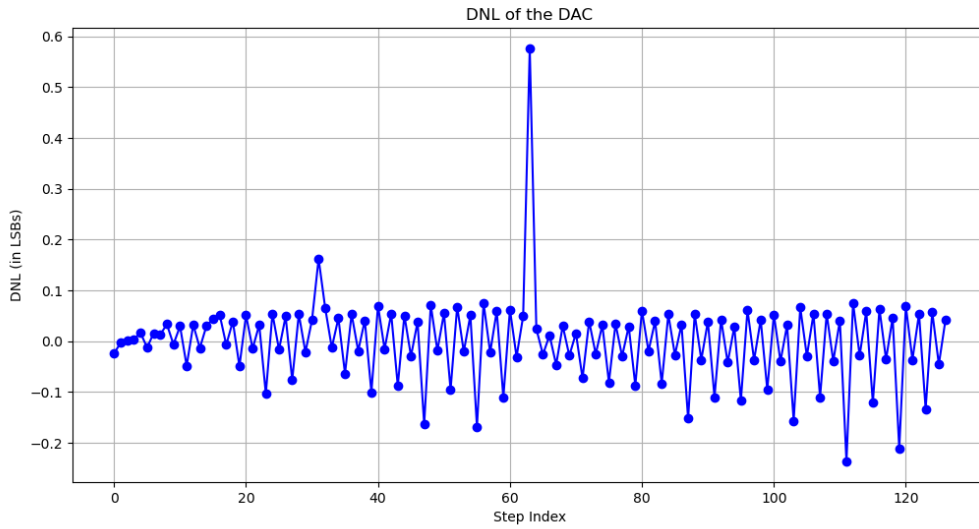


Figure 10: DNL of the DAC in ideal conditions. The worst case DNL is below 0.6 LSBs, which meets the design requirement of less than 2 LSBs.

## 6.3 Integral Non-linearity

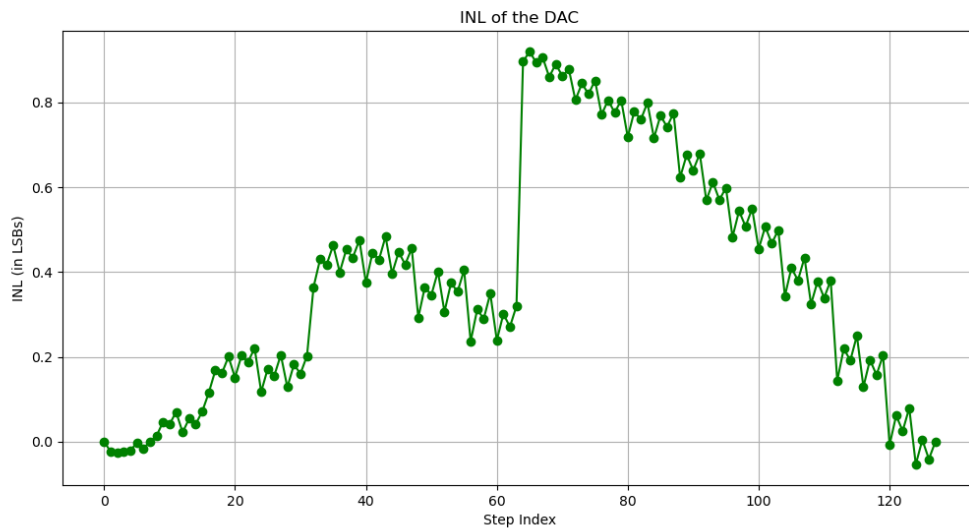


Figure 11: INL of the DAC in ideal conditions. The INL is below 1 LSB, which meets the design specifications given to us of 4 LSBs.

## 6.4 Sweep of Output Current vs Output Voltage

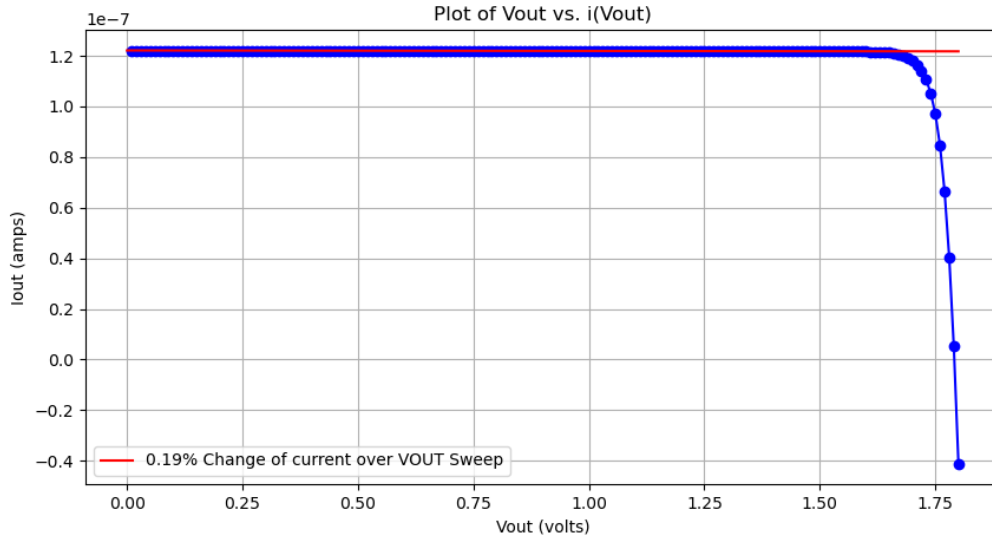


Figure 12: This is the output current vs output voltage sweep plot. The Voltage change for 80 percent of the power supply is 0.19 percent per Volt, which meets the requirement of 0.5 percent current change per volt.

## 7 Monte Carlo Simulations

### 7.1 Voltage Current Characteristics

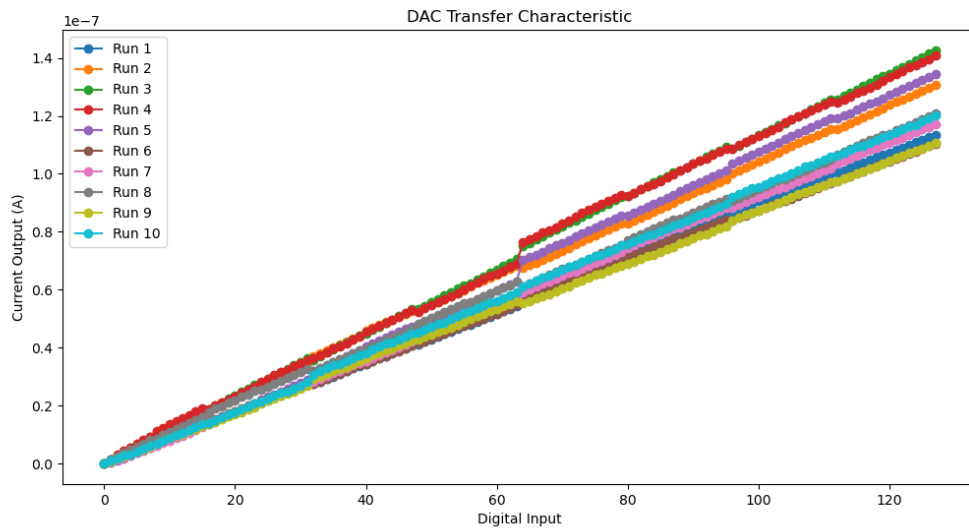


Figure 13: Voltage Current Characteristic of our DAC under Monte Carlo Simulation



## 7.2 DNL

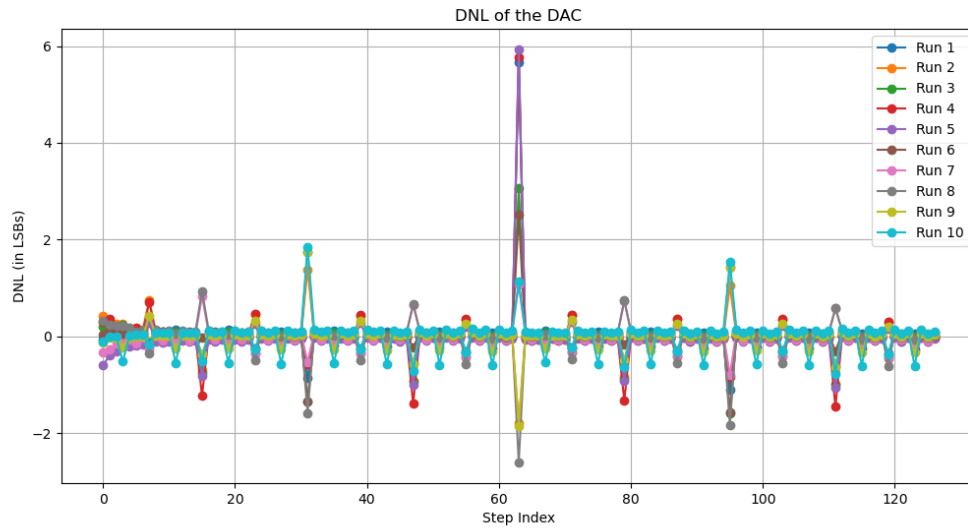


Figure 14: DNL of our DAC through Monte Carlo Simulations. The worst case DNL is around 6 LSBs, which meets the performance specifications of 8.

## 7.3 INL

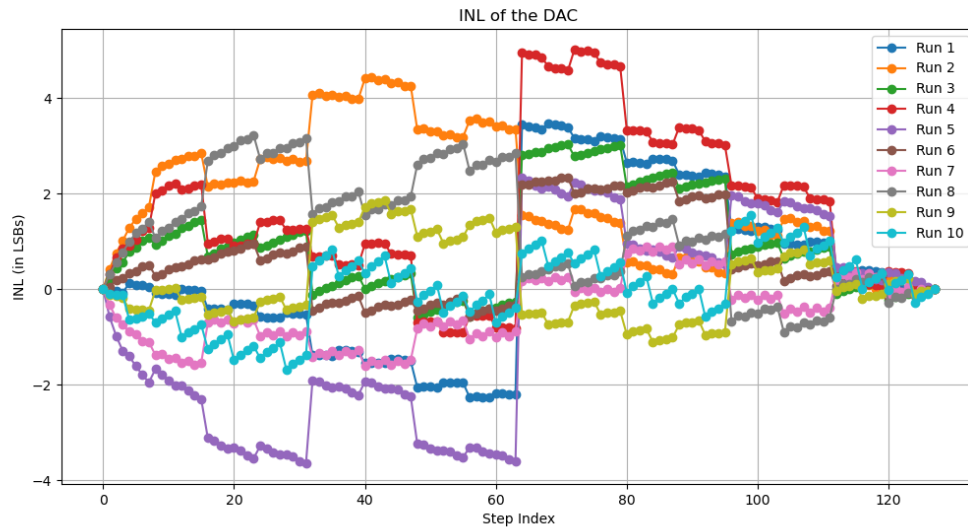


Figure 15: INL of our DAC through Monte Carlo Simulations. The INL is around 5 LSBs, which meets the performance specification of a worst case INL of 8.

## 8 Layout

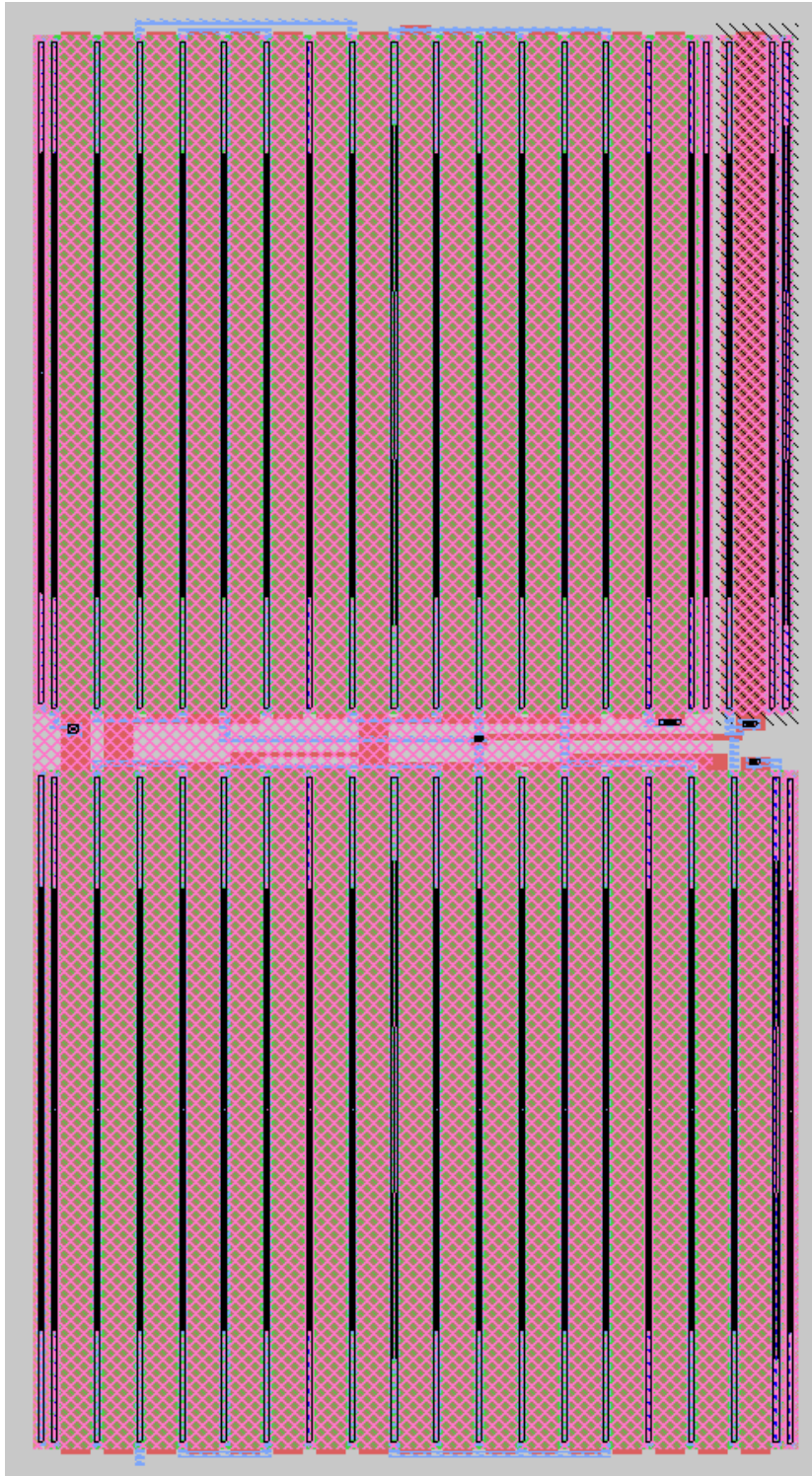


Figure 16: Layout of DAC ladder network



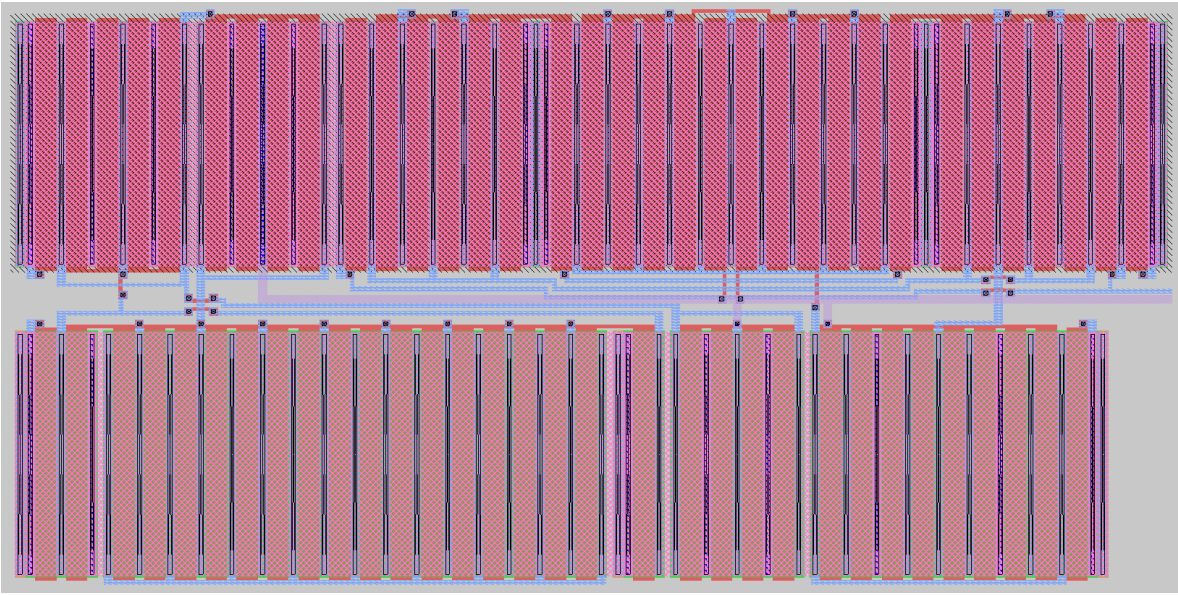


Figure 17: Combined layout of output current mirror and supply-independent voltage bias generator

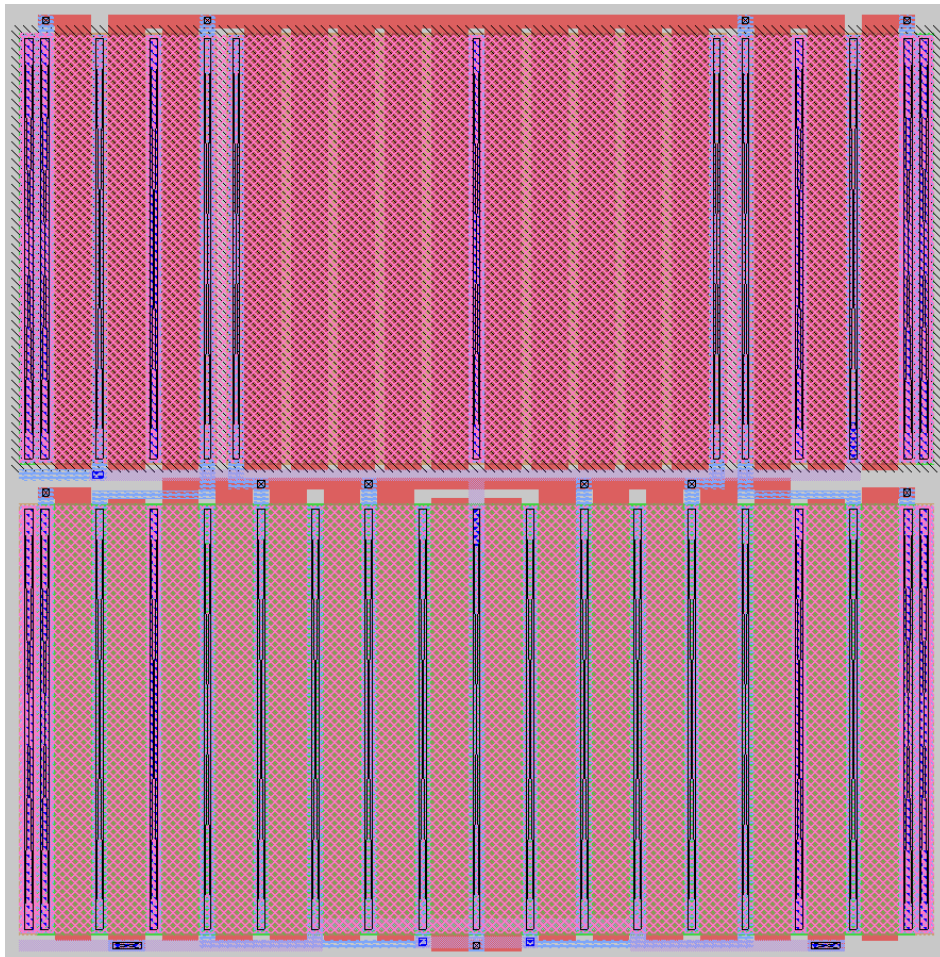


Figure 18: Layout of cascode bias-voltage generator



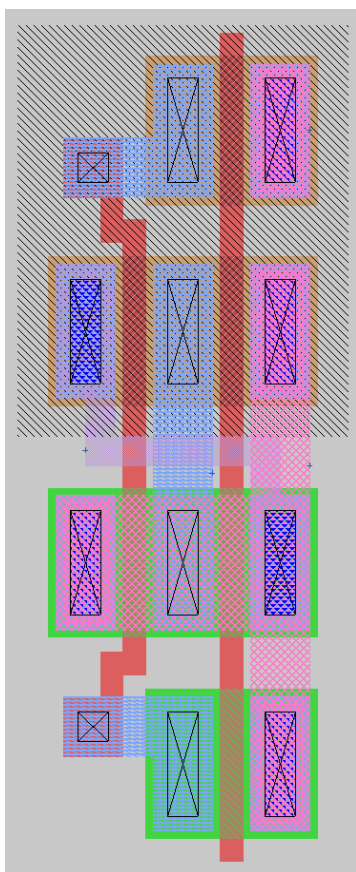


Figure 19: Layout of a single multiplexer

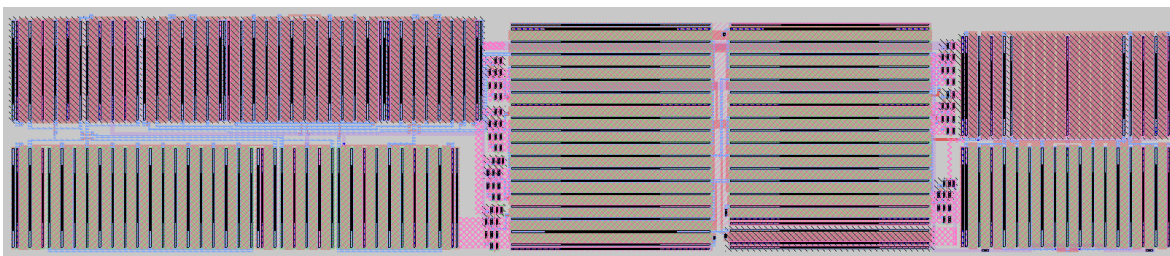


Figure 20: Layout of full DAC design

## 9 Layout Versus Schematic

Circuit 1 cell sky130\_fd\_pr\_\_pfet\_01v8 and Circuit 2 cell sky130\_fd\_pr\_\_pfet\_01v8 are black boxes.  
Equate elements: no current cell.

Device classes sky130\_fd\_pr\_\_pfet\_01v8 and sky130\_fd\_pr\_\_pfet\_01v8 are equivalent.

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Equate elements: no current cell.

Device classes sky130\_fd\_pr\_\_nfet\_01v8 and sky130\_fd\_pr\_\_nfet\_01v8 are equivalent.

Flattening unmatched subcell mux in circuit lds\_for\_lvs.spice (0)(7 instances)

Flattening unmatched subcell dac in circuit dac\_top.spice (1)(1 instance)

Flattening unmatched subcell big in circuit dac\_top.spice (1)(1 instance)

Flattening unmatched subcell cascode\_biasgen in circuit dac\_top.spice (1)(1 instance)

Flattening unmatched subcell mux\_tall in circuit dac\_top.spice (1)(7 instances)

Class lds\_for\_lvs.spice (0): Merged 62 parallel devices.

Class dac\_top.spice (1): Merged 62 parallel devices.

Subcircuit summary:

Circuit 1: lds_for_lvs.spice	Circuit 2: dac_top.spice
sky130_fd_pr__pfet_01v8 (72->47)	sky130_fd_pr__pfet_01v8 (72->47)
sky130_fd_pr__nfet_01v8 (101->64)	sky130_fd_pr__nfet_01v8 (101->64)
Number of devices: 111	Number of devices: 111
Number of nets: 58	Number of nets: 58

Resolving symmetries by property value.

Resolving symmetries by pin name.

Netlists match with 15 symmetries.

Cells have no pins; pin matching not needed.

Device classes lds\_for\_lvs.spice and dac\_top.spice are equivalent.

Final result: Circuits match uniquely.

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