MADVLSI MP3 Report

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1 Introduction

The goal of this project was to design a folded-cascode differential amplifier and its associated bias circuit using Xschem, Magic and Skywater Technology's sky130 PDK.

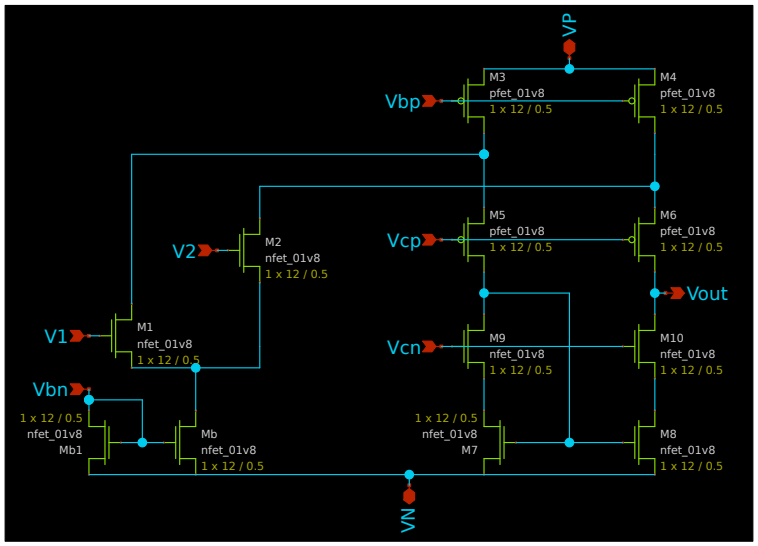

Figure 1: Basic schematic of a folded-cascode differential amplifier.

1.1 Design Files

The design files for this project can be found here: https://github.com/kburp/folded-cascode-diffamp-vlsi

2 Circuit Analysis

a) Which input voltage is the non-inverting input? Which is the inverting input?

$I_{out} = I_6 - I_{10}$ by KCL
$I_{10} = I_9$ because of the low-voltage current mirror
$I_{out} = I_6 - I_9$ by substitution
$I_6 = I_b - I_2$ and $I_9 = I_b - I_1$ by KCL
$I_{out} = I_b - I_2 - (I_b - I_1)$ by substitution
$I_{out} = I_1 - I_2$
I_1 and I_2 are dependent on V_1 and V_2 respectively
Therefore, V_1 is the non-inverting input and V_2 is the inverting input

b) What is the allowable common-mode input voltage range of this circuit?

For a common-mode voltage input, we assume $V_1 = V_2 = V_{cm}$. Under this condition, since M_1 and M_2 share a common gate and source and $I_1 + I_2 = I_b$ by KCL, the differential pair comprised of M_1, M_2, and M_b can be collapsed into an equivalent source follower M_{sf} and M_b where the two transistors have the same channel current I_b. M_{sf} has gate voltage V_{cm}, M_b has gate voltage V_{bn}, and the two transistors have a common source/drain voltage V. Since M_b has to be saturated in order to maintain a constant channel current, M_{sf} must also be saturated because it has the same current through it and the transistors are matching. Using the EKV model, the current through each transistor is:

$M_{sf} \Rightarrow I_b = SI_s log^2(1 + e^{\kappa((V_{cm} - V_{T0}) - V)/2U_T})$
$M_b \Rightarrow I_b = SI_s log^2(1 + e^{\kappa(V_{bn} - V_{T0})/2U_T})$

Setting the two currents equal to each other and simplifying results in

$\kappa \cdot V_{cm} - V = \kappa \cdot V_{bn}$
$V = \kappa(V_{cm} - V_{bn})$

To keep M_b in saturation, $V \geq V_{DSsat}$, so

$\kappa(V_{cm} - V_{bn}) \geq V_{DSsat}$
$V_{cm} \geq V_{bn} + \frac{V_{DSsat}}{\kappa}$

The upper bound of V_{cm} is V_{DD}.

c) If the output voltage were fixed by a voltage source somewhere in the middle of the rails, what would be the output current in terms of I1 and I2 if the Early effect were negligible?

See answer to question A for derivation.

d) Do we need to make the bias current sourced by M3 and M4 equal to the diff pair bias current, I_b?

I_3 and I_4 should be equal to I_b. With a large differential mode input to the circuit, $I_1 >> I_2$ or $I_1 << I_2$, and the larger of the currents will approximately equal I_b by KCL. If I_3 and I_4 are smaller than I_b, I_b becomes limited by I_3 or I_4 and M_b can no longer be in saturation. If I_3 and I_4 are larger than I_b, this results in excess power dissipation. Since I_{out} only depends on I_1 and I_2, the current I_3 and I_4 excess of I_b will be sunk into ground, resulting in the circuit using more power than it requires.

e) Design a bias circuit for the folded-cascode amplifier that receives input from a single current source, I_b, and generates cascode bias voltages, V_{cn} and V_{cp}, optimally for a given bias current I_b so as to maximize the output voltage swing of the amplifier. Your circuit must also generate the other bias voltages, V_{bn} and V_{bp}, so that $I_3 = I_4 = I_b$.

My bias circuit is equivalent to twelve transistors shown in the schematic below. The circuit can be broken into two main parts. The left half uses V_{bn}, generated by a diode-connected nMOS transistor with I_b fed into it (not shown in this schematic), and generates V_{cp}. The right half uses V_{bn} to generate V_{bp} and V_{cn}. M_1 through M_5 is the same circuit as M_6 through M_{10}, except the pMOS and nMOS transistors are switched.

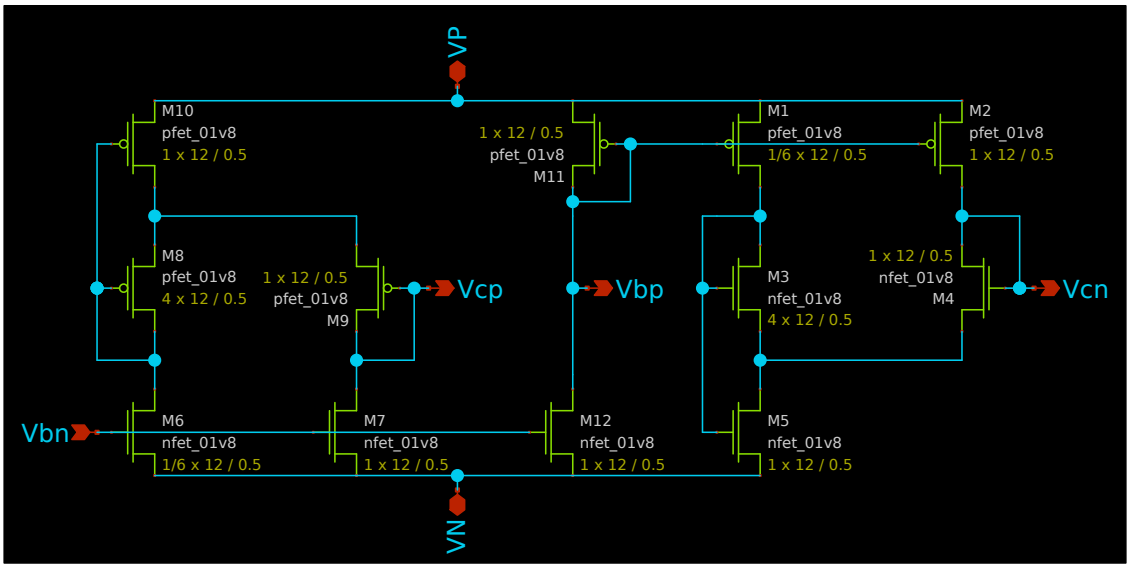

Figure 2: Basic schematic of the bias circuit.

The goal of the bias circuit is to generate four bias voltages such that each one keeps the transistors in the main amplifier in saturation. Taking the right side of the circuit as an example, Since M_{11} is diode-connected, it is in saturation, so a current mirror composed of M_{11} and another pMOS transistor produces a saturation current on the output. From this, we know that a pMOS transistor with its source at V_{DD} and its gate at V_{bp} will be saturated, so V_{bp} is a sufficient bias voltage for M_3 and M_4 in the main part of the amplifier.

Continuing analysis on the right side of the bias circuit, we know that M_3 is saturated because it is diode-connected, but M_5 could be operating in the ohmic region. If M_3 and M_5 have multiplicities m_3 and 1 respectively, their gate voltage is V_G, and their common source/drain voltage is V, their currents can are given by

$$
\begin{aligned}
I_3 &= I_1 = m_3 I_s f(V_G, V) \\
I_5 &= I_1 + I_2 = I_s(f(V_G, 0) - f(V_G, V)) \\
I_1 + I_2 + \tfrac{I_1}{m_3} &= I_s f(V_G, 0)
\end{aligned}
$$

Using this, the saturation index (ratio of forward and reverse current) of M_5 is given by

$$\frac{I_F}{I_R} = \frac{f(V_G,0)}{f(V_G,V)} = \frac{I_1+I_2+(I_1/m_3)}{I_1/m_3} = \frac{m_3 I_2}{I_1} + m_3 + 1$$

We want M_5 to be in saturation becuase this would guarantee that V, which is used to generate V_{cn}, would be greater than or equal to V_{DSsat}, making a transistor with drain voltage V and its source at ground saturated. Since V_{cn} is a cascoded bias voltage, we want to generate a gate voltage that can put an nMOS transistor whose source is at V_{DSsat} in saturation. Putting a diode-connected transistor M_4 in the circuit with gate voltage V_{cn} and source voltage V accomplishes this. If the saturation index of M_5 is in the range of 20 to 30, we can say that M_5 will be saturated. If we let the current ratio $\frac{I_2}{I_1} = n$, the saturation index becomes

$$20 \leq m_3 \cdot n + m_3 + 1 \leq 30$$

To make the number of transistors in the layout match nicely, we can let $n = m_3 + 2$. Making m_3 an even number also optimizes the layout, so solving the equation, we find that $m_3 = 4$ and $n = 6$ is a solution. m_3 can be implemented by making the multiplicity of M_3 equal to 4 and M_5 equal to 1, and n can be implemented by making the multiplicity of M_1 equal to $\frac{1}{6}$ and M_2 equal to 1.

A similar analysis of the left side of the circuit yields the same multiplicities for the complementary circuit.

3 Schematic Capture and Simulation

After creating the basic schematics, the next step is to turn them into layout-driven schematics that can be referenced during the layout process. The layout-driven schematics of both the main part of the amplifier and the bias circuit create common centroids for matching transistors by splitting each transistor into multiple transistors that are less wide. The outside edges of the circuit also contain dummy devices to maintain the same surroundings for all of the active transistors.

3.1 Layout-Driven Schematics

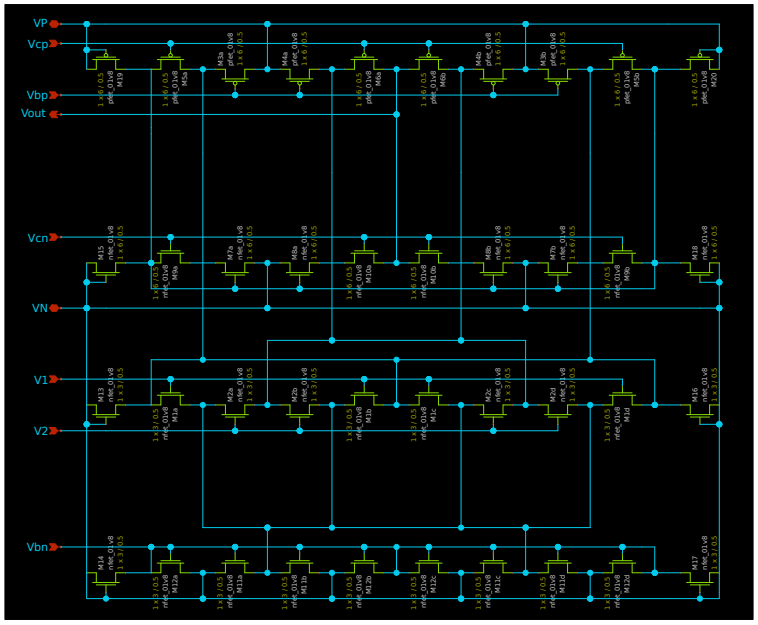

Figure 3: Layout-driven schematic of the main part of the amplifier. The top two rows of transistors have a width of $6\mu m$ and the bottom two rows of transistors have a width of $3\mu m$.

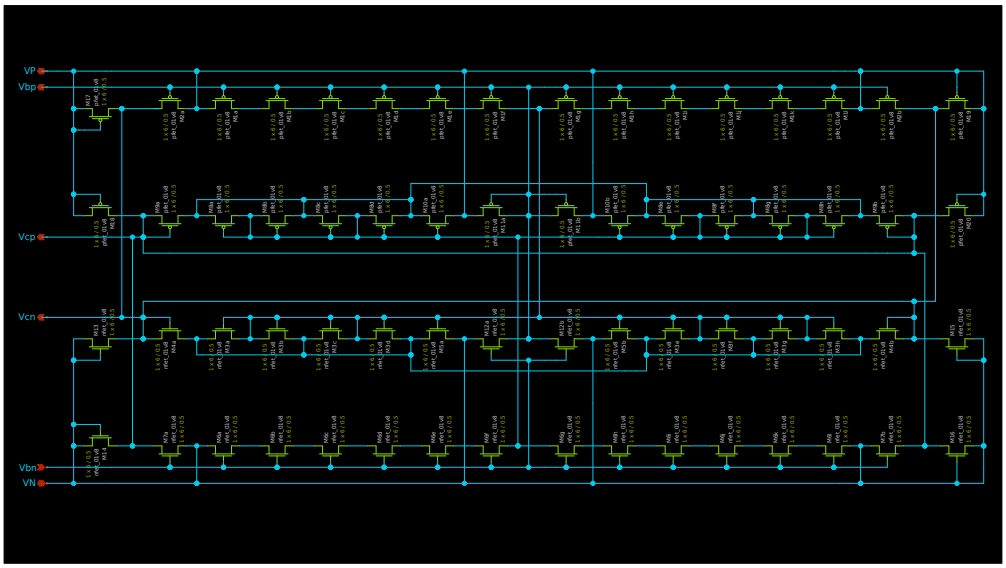

Figure 4: Layout-driven schematic of the bias circuit. All of the transistors have a width of $6\mu m$.

3.2 Voltage Transfer Characteristics

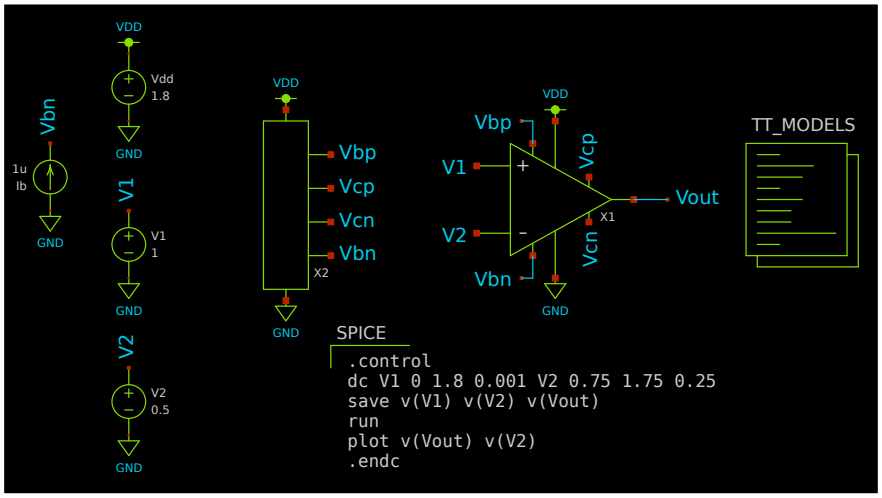

Figure 5: Schematic of VTC test harness.

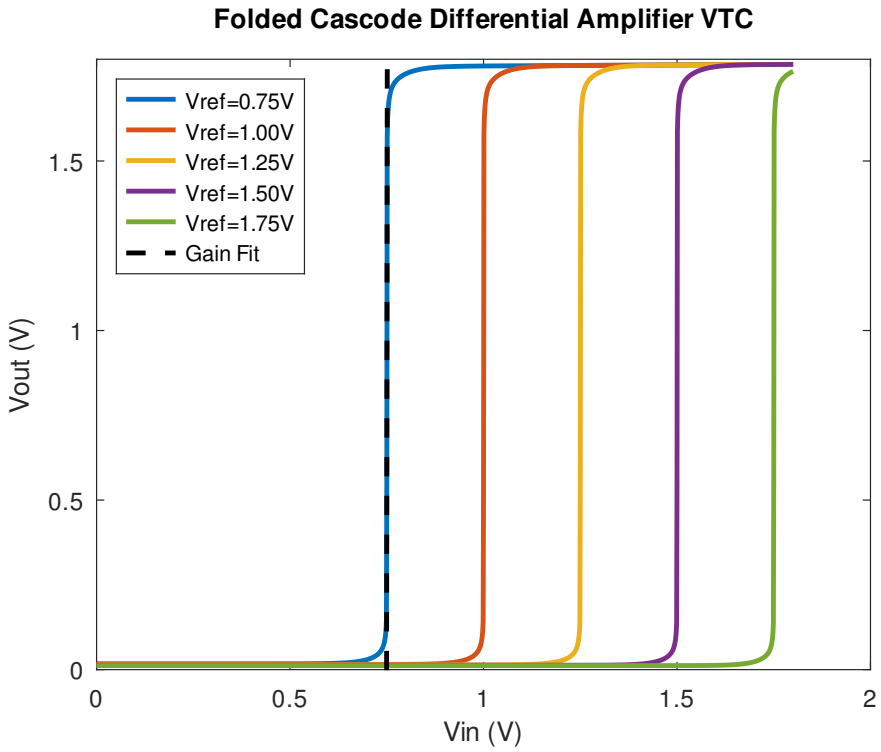

Figure 6: The amplifier's VTC for five different values of the inverting input. The slope of the curves is the DC gain of the amplifier.

The DC gain of the circuit, found from the slope of the VTC, is around 1020.

3.3 Voltage-to-Current Transfer Characteristics

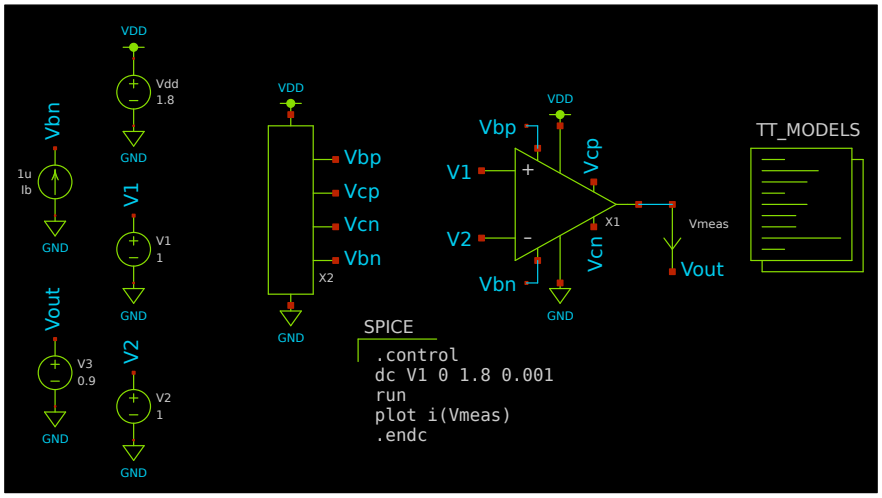

Figure 7: Schematic of IV characteristic test harness.

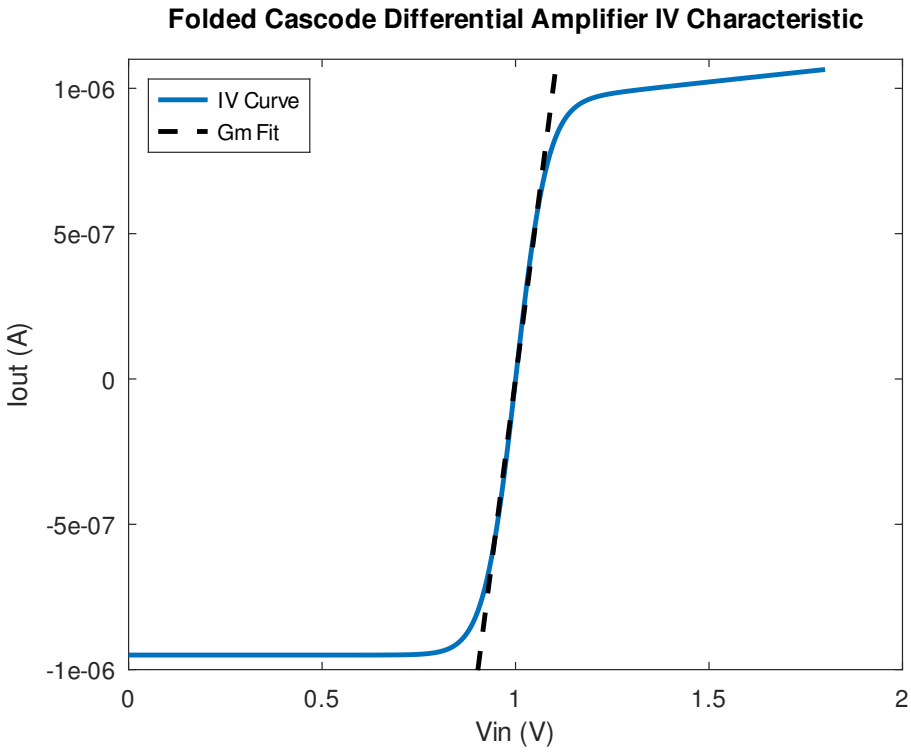

Figure 8: IV characteristic of the folded-cascode differential amplifier when the inverting input is held at 1V and the output is held at 0.9V. The slope of the curve is the incremental transconductance gain of the circuit.

From the slope of the voltage-to-current transfer characteristic, the incremental transconductance gain of the circuit is 1.03e-5 mhos. The limiting values of the output current are $1.06\mu A$ at V_{DD} and $-0.950\mu A$ at ground.

3.4 Loopgain

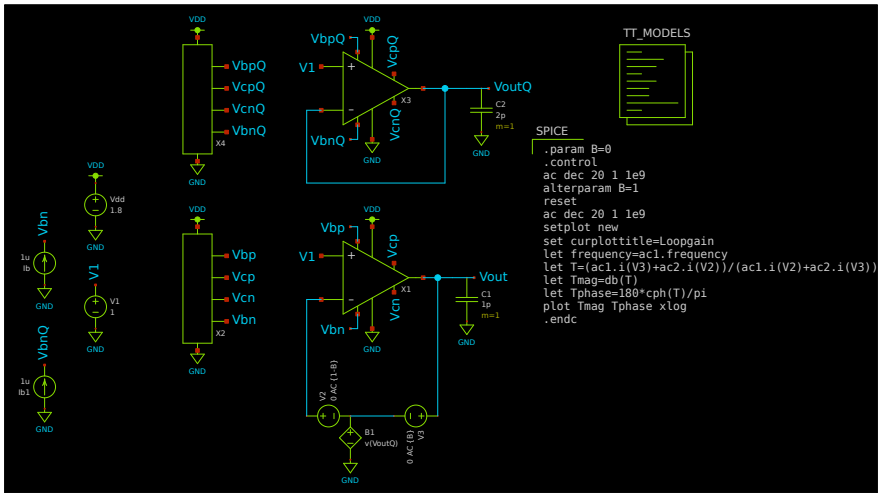

Figure 9: Schematic of loopgain test harness.

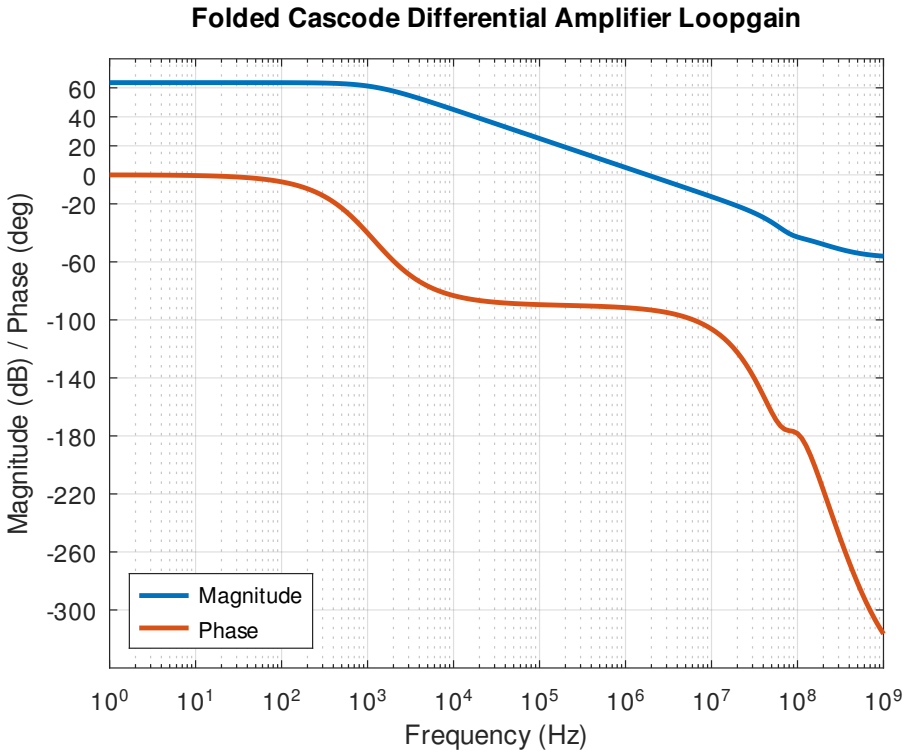

Figure 10: Magnitude and phase of the loopgain of the amplifier. The loopgain was found using Ochoa's Z method, which involves performing AC simulations with two voltage sources and calculating the ratio between the current in each voltage source due to the other voltage source and the current through each voltage source due to itself.

The low-frequency gain is 63.581dB, which is equal to 1510. This is greater than the DC gain calculated from the VTC. The unity-gain crossover frequency is 1.78MHz. Using the load capacitance of 2pF and incremental transconductance gain of 1.03e-5, the expected unity-gain crossover frequency is $\frac{Gm}{2\pi C} = 819\text{kHz}$.

3.5 Unity-Gain Follower Frequency Response

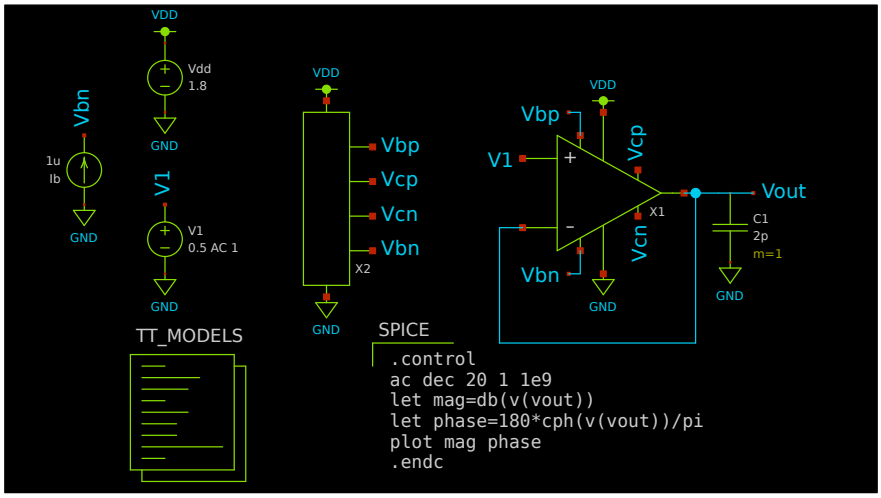

Figure 11: Schematic of frequency response test harness.

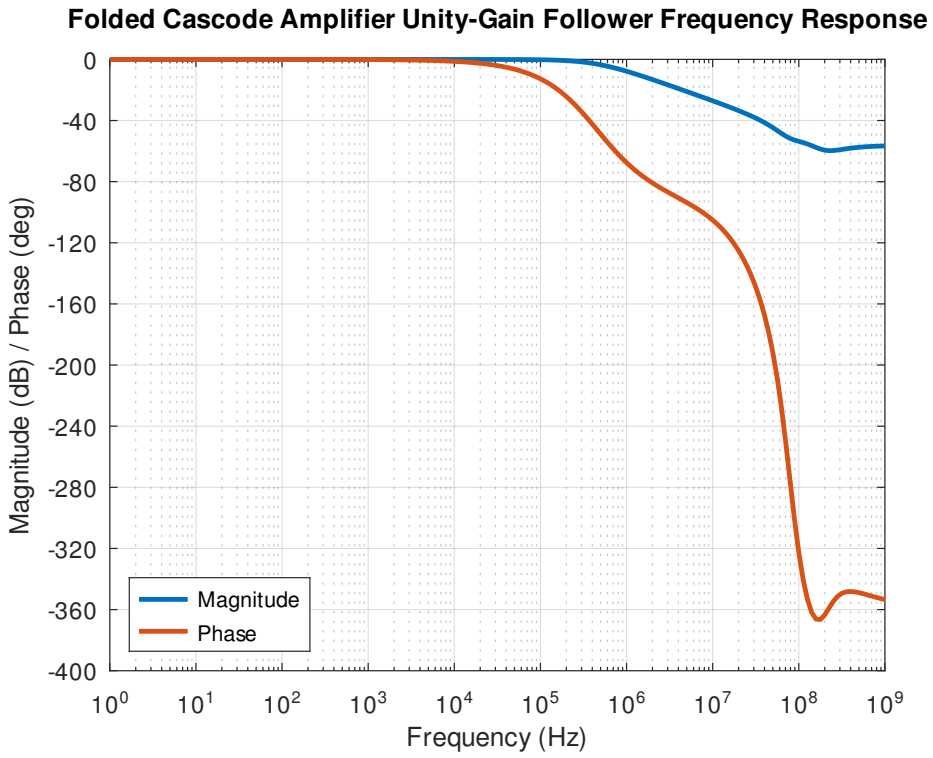

Figure 12: Unity-gain frequency response of the amplifier found by performing an AC sweep.

The corner frequency of the circuit is 447kHz. This is lower than the measured unity-gain crossover frequency of the loopgain by about a factor of 4.

4 Layout Design

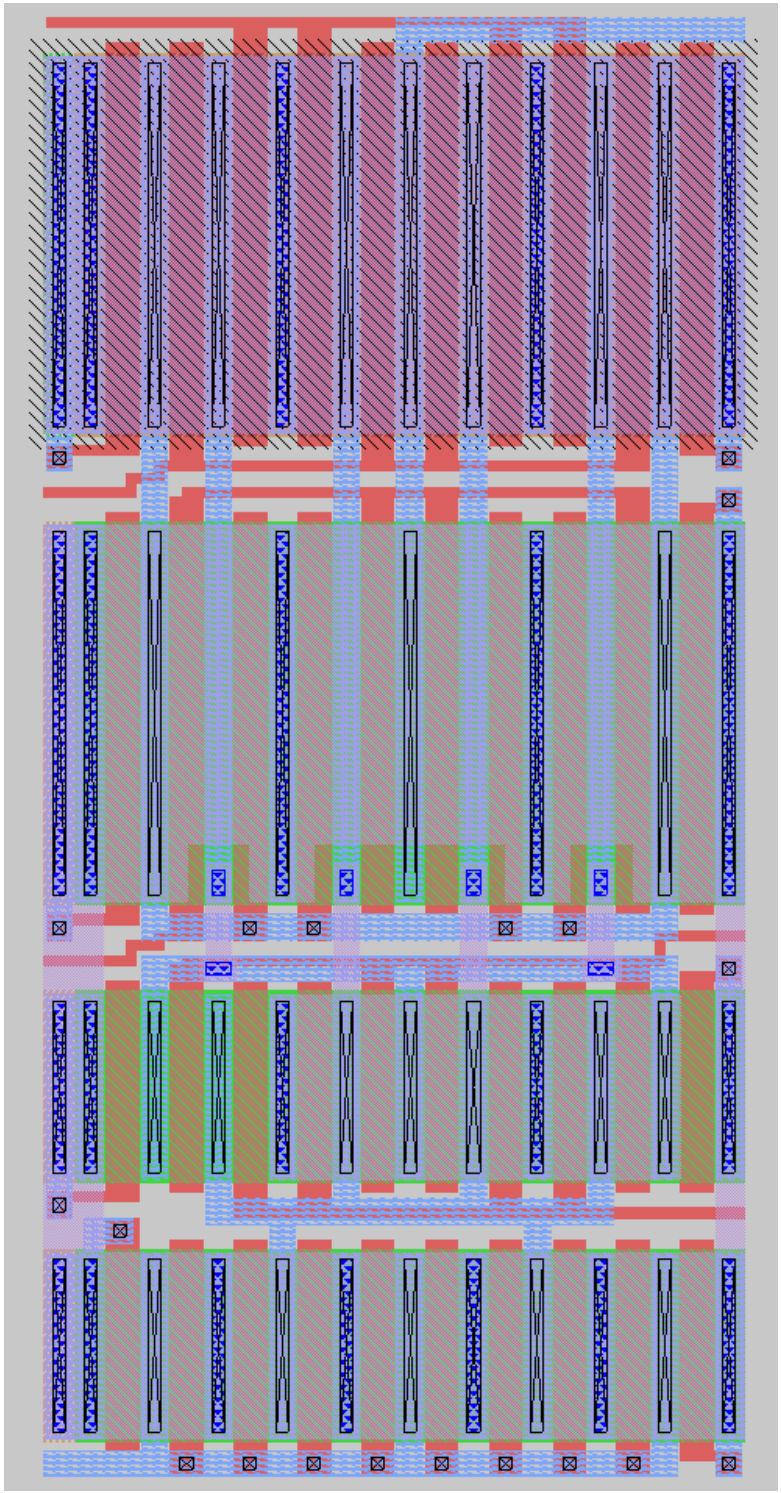

Figure 13: Layout of the main part of the amplifier designed in Magic. The output voltage is available at the top right of the circuit in the local interconnect layer, and the differential pair inputs are also available on the right side in the polysilicon layer.

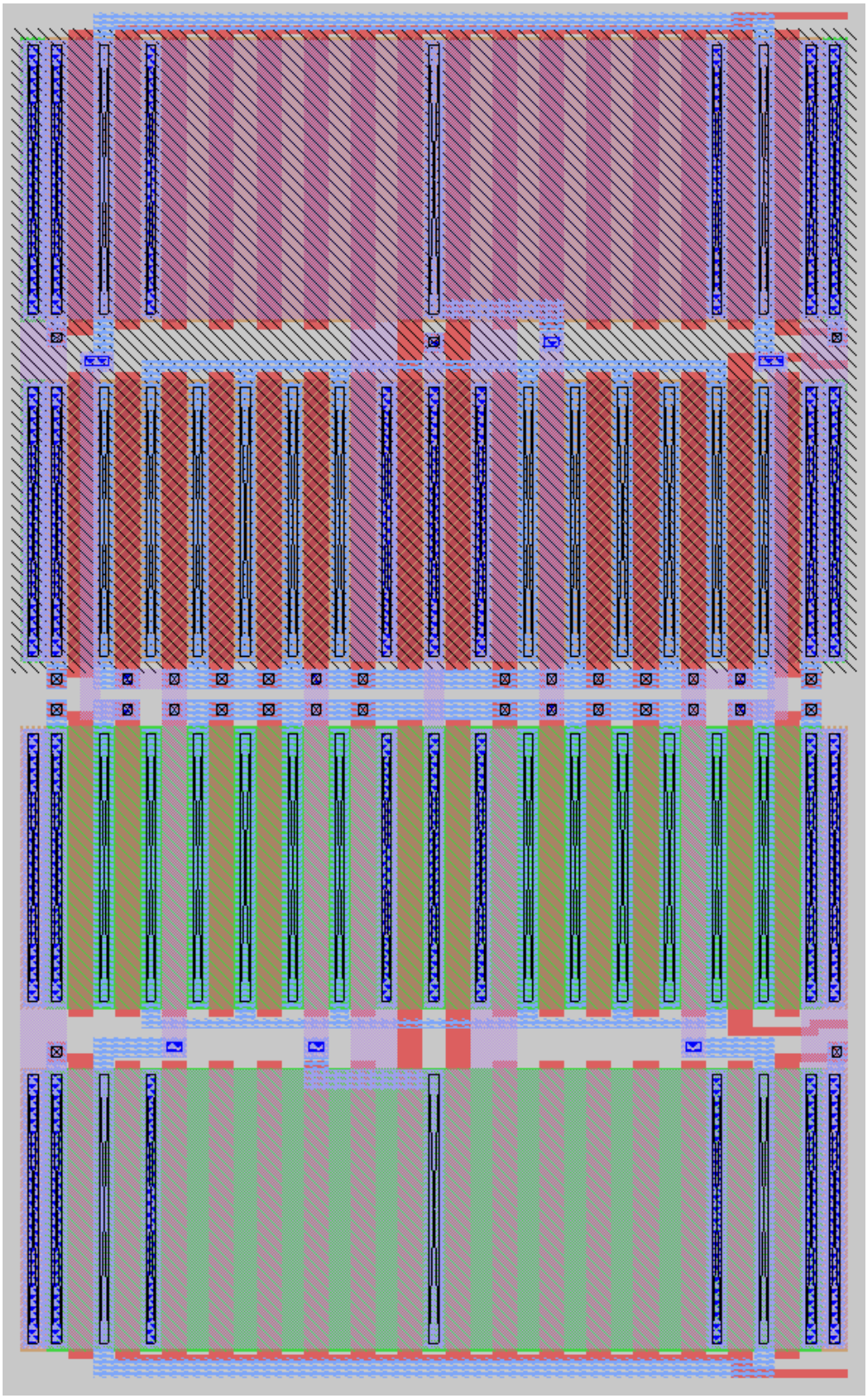

Figure 14: Layout of the bias circuit designed in Magic. The four bias voltages are available as outputs on the polysilicon layer on the rights side of the circuit.

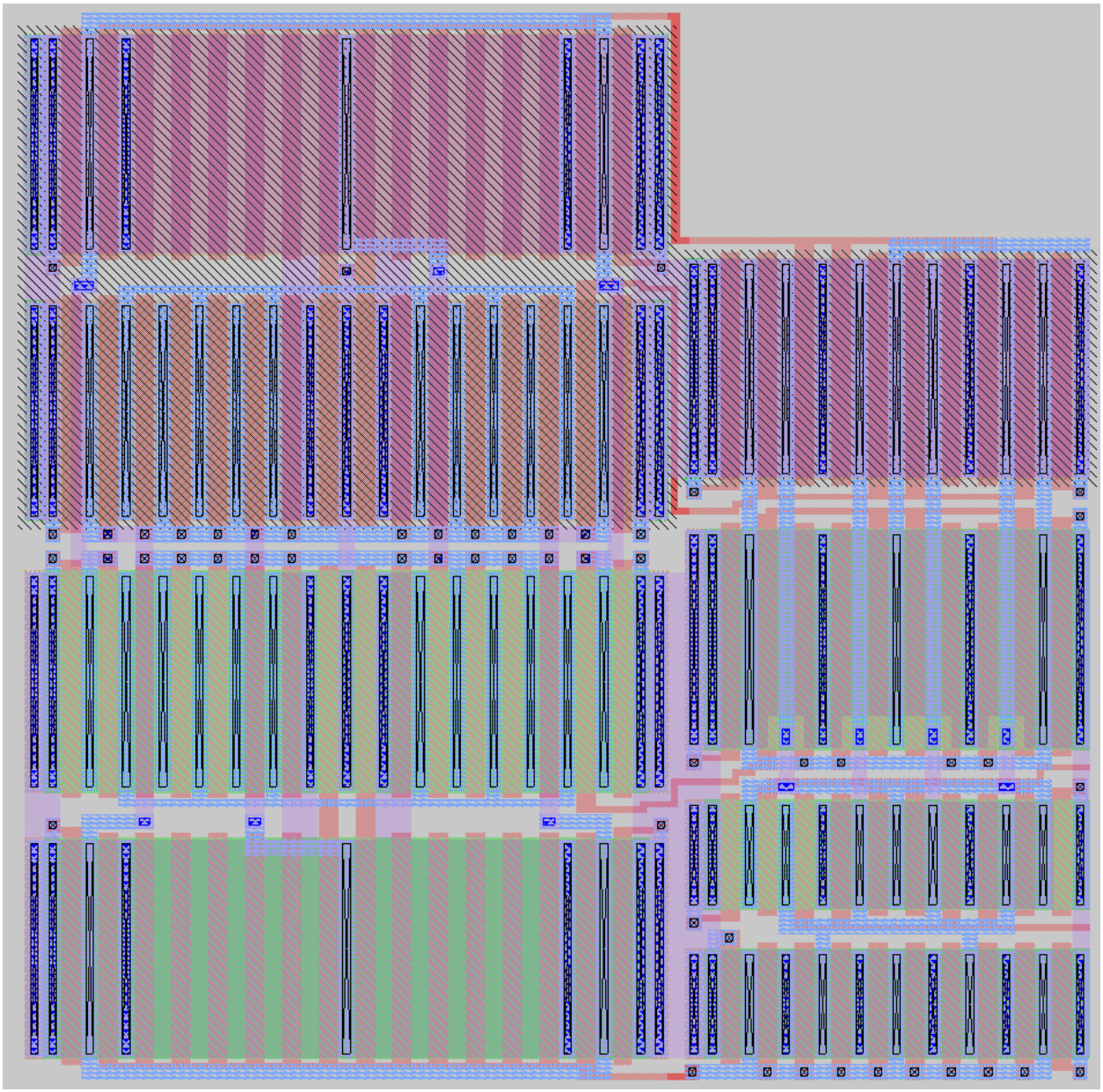

Figure 15: Full layout of the folded-cascode differential amplifier and its bias circuit.

5 Layout Versus Schematic

A layout versus schematic comparison using Netgen shows that the layout and schematic SPICE netlists match.

```
Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.
Flattening unmatched subcell biasgen_lds in circuit fc_diffamp_full_xschem.spice (0)(1 instance)
Flattening unmatched subcell fc_diffamp_lds in circuit fc_diffamp_full_xschem.spice (0)(1 instance)
Flattening unmatched subcell biasgen in circuit full_fc_diffamp.spice (1)(1 instance)
Flattening unmatched subcell fc_diffamp in circuit full_fc_diffamp.spice (1)(1 instance)

Class fc_diffamp_full_xschem.spice (0):  Merged 46 parallel devices.
Class full_fc_diffamp.spice (1):  Merged 46 parallel devices.
Subcircuit summary:
Circuit 1: fc_diffamp_full_xschem.spice    |Circuit 2: full_fc_diffamp.spice
-------------------------------------------|-------------------------------------------
sky130_fd_pr__pfet_01v8 (42->24)           |sky130_fd_pr__pfet_01v8 (42->24)
sky130_fd_pr__nfet_01v8 (62->34)           |sky130_fd_pr__nfet_01v8 (62->34)
Number of devices: 58                      |Number of devices: 58
Number of nets: 41                         |Number of nets: 41
-----------------------------------------------------------------------------------------
Resolving symmetries by property value.
Resolving symmetries by pin name.
Netlists match with 28 symmetries.
Cells have no pins;  pin matching not needed.
Device classes fc_diffamp_full_xschem.spice and full_fc_diffamp.spice are equivalent.

Final result: Circuits match uniquely.
```