MADVLSI MP2 Report

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1 Introduction

The goal of this project was to create a schematic, layout, and layout vs. schematic comparison for a four-bit shift register composed of D flip-flops that use complementary set-reset logic (CSRL).

1.1 Design Files

The design files for this project can be found here: https://github.com/kburp/four-bit-shift-register-vlsi

2 Schematic Capture and Simulation

2.1 CSRL D Flip-flop

The first step in creating a four-bit shift register is to create a transistor-level schematic for a CSRL D flip-flop using Xschem. The CSRL D flip-flop can be made with fourteen transistors, but in order to make the layout easier, the pMOS transistor above the bi-stable element on the right was split into two transistors (M5 and M6). All of the transistors have a strength ratio of 1, except for the nMOS transistor below the bi-stable element on the left (M15), which has a strength ratio of 4.

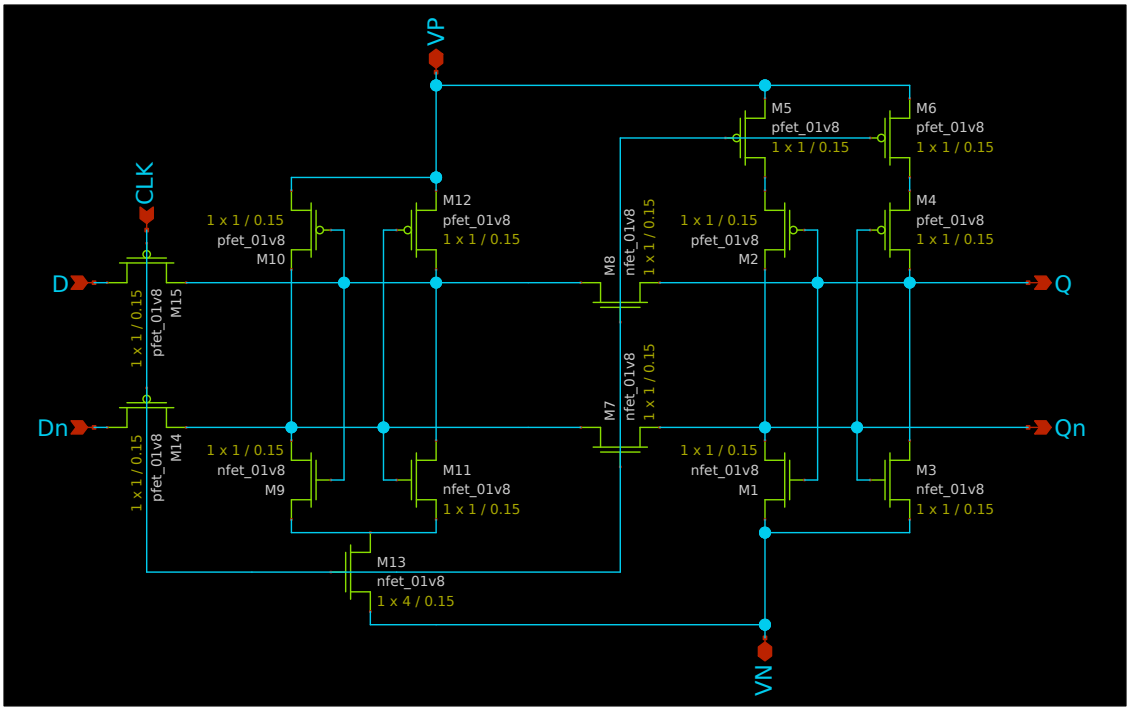

Figure 1: Transistor-level CSRL D Flip-flop schematic.

2.2 Four-bit Shift Register

An inverter and four D flip-flops can be cascaded to create a four-bit shift register.

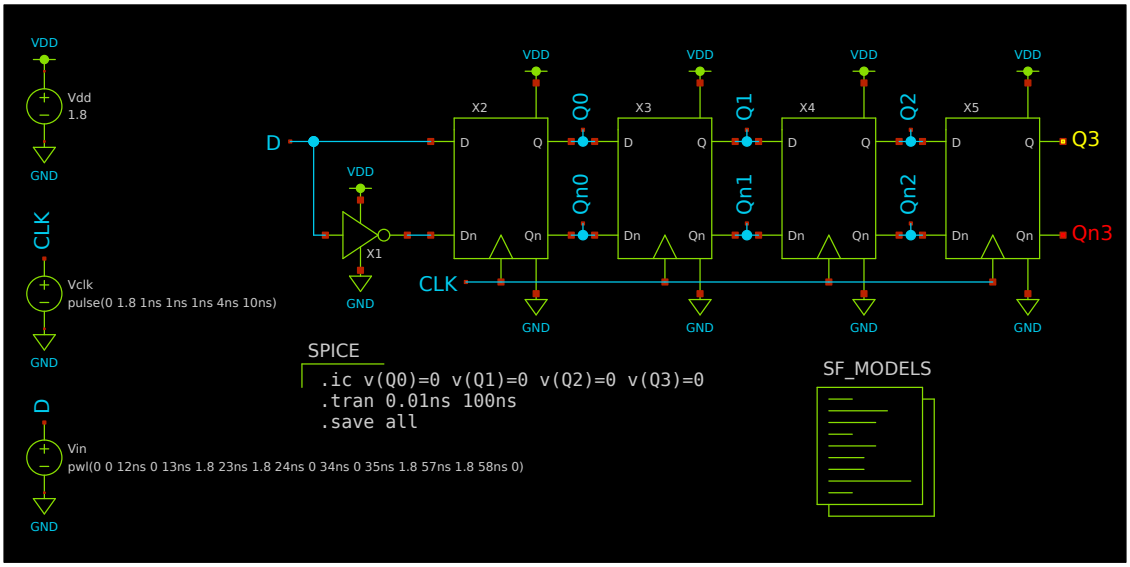

Figure 2: Schematic for simulation of four-bit shift register.

2.3 Transient Simulation

The transient simulation results show that the shift register works as intended. Figure 3 shows plots of voltages at various nets in the circuit alongside the clock signal. Since the flip-flops are rising edge-triggered, it is expected that the flip-flops change output on the rising edge of the clock. The top panel with the plot of the signal D shows that D is low at the start of the first two clock cycles, then goes high before the rising edge of the third cycle. The second panel plotting Q0 (red) shows that on the rising edge of the third cycle, the output of the first register becomes a weak 1, and it becomes a strong 1 on the falling edge of the same clock cycle. Since D is low on the next rising edge, Q0 also goes low on the fourth cycle. D goes high for the following two cycles and then goes low for the rest of the simulation, which is reflected in the output of the first register. The bottom three panels, which contain plots of Q1, Q2, and Q3, show that the output of each register reflects the output of the previous register delayed by one clock cycle.

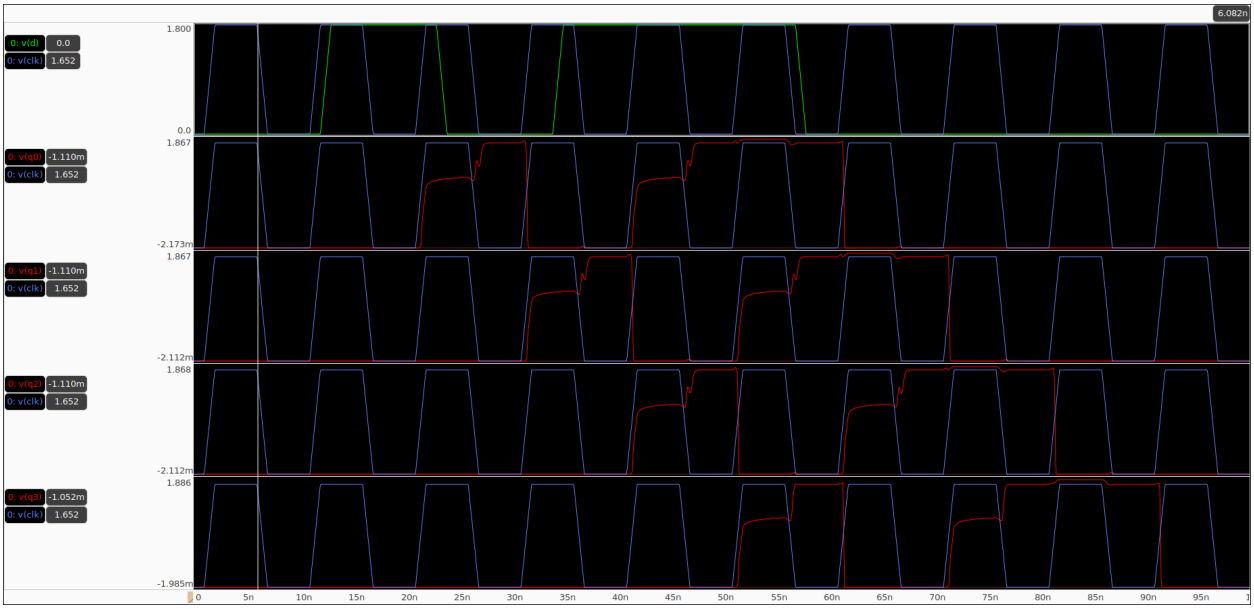

Figure 3: Voltages at D (green), Q0, Q1, Q2, and Q3 (red), each plotted over CLK (blue).

The plots of Q and Qn for each of the registers also show that the outputs of the registers are as expected. For each of the registers, Qn has the complementary output of Q.

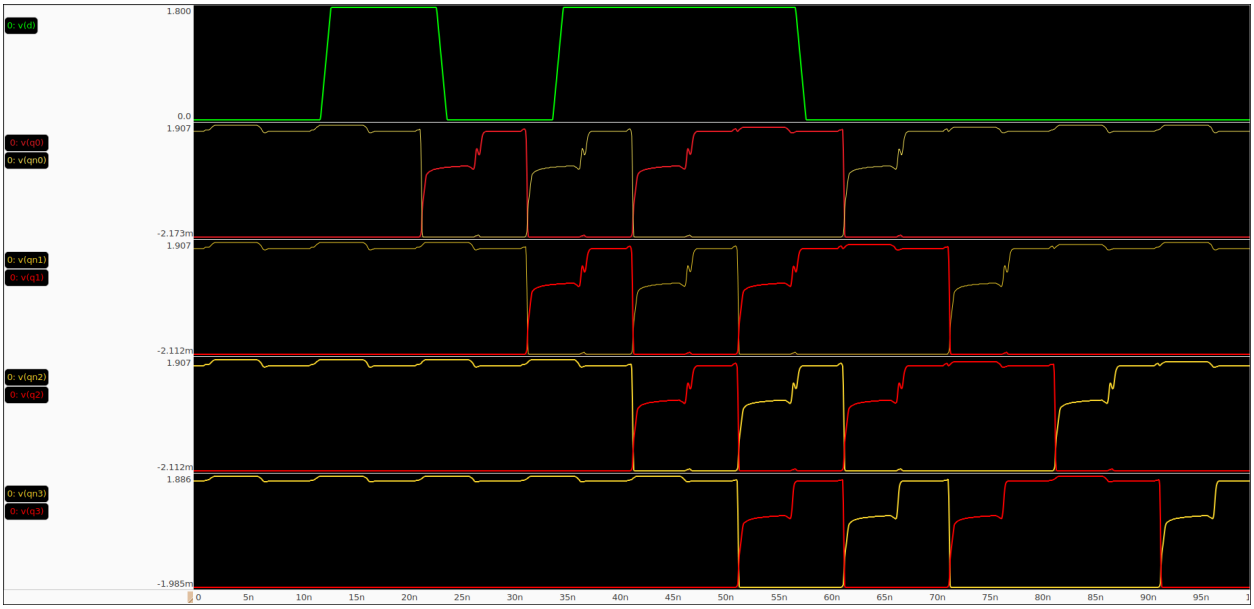

Figure 4: The outputs Q (red) and Qn (yellow) for each of the four flip-flops.

3 Layout Design

The layout of the four-bit shift register was designed using Magic.

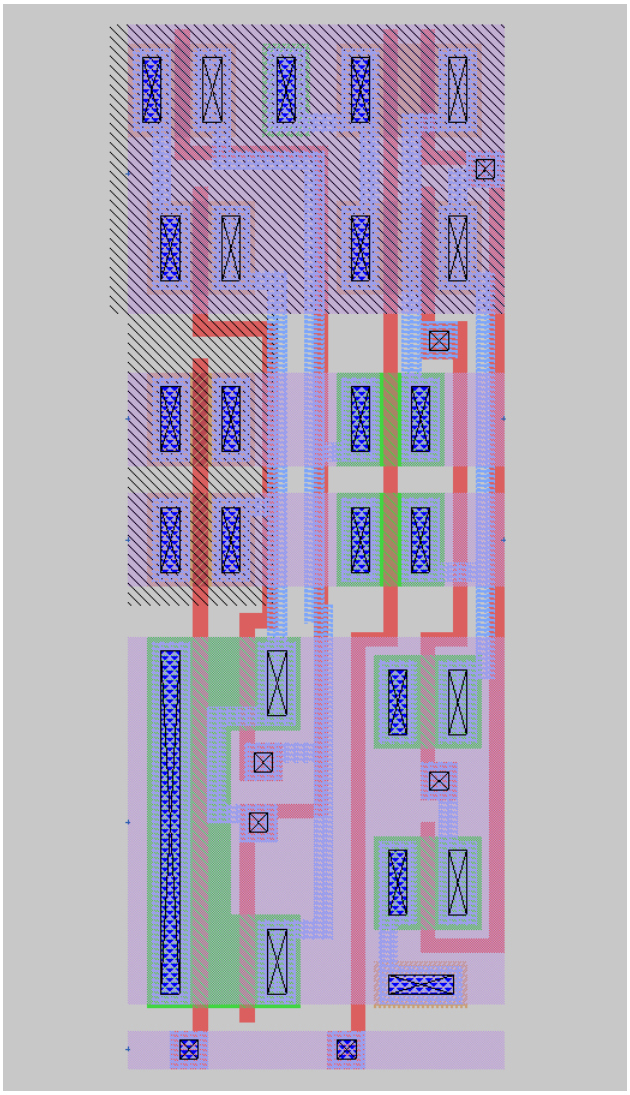

Figure 5: CSRL D flip-flop layout using Magic.

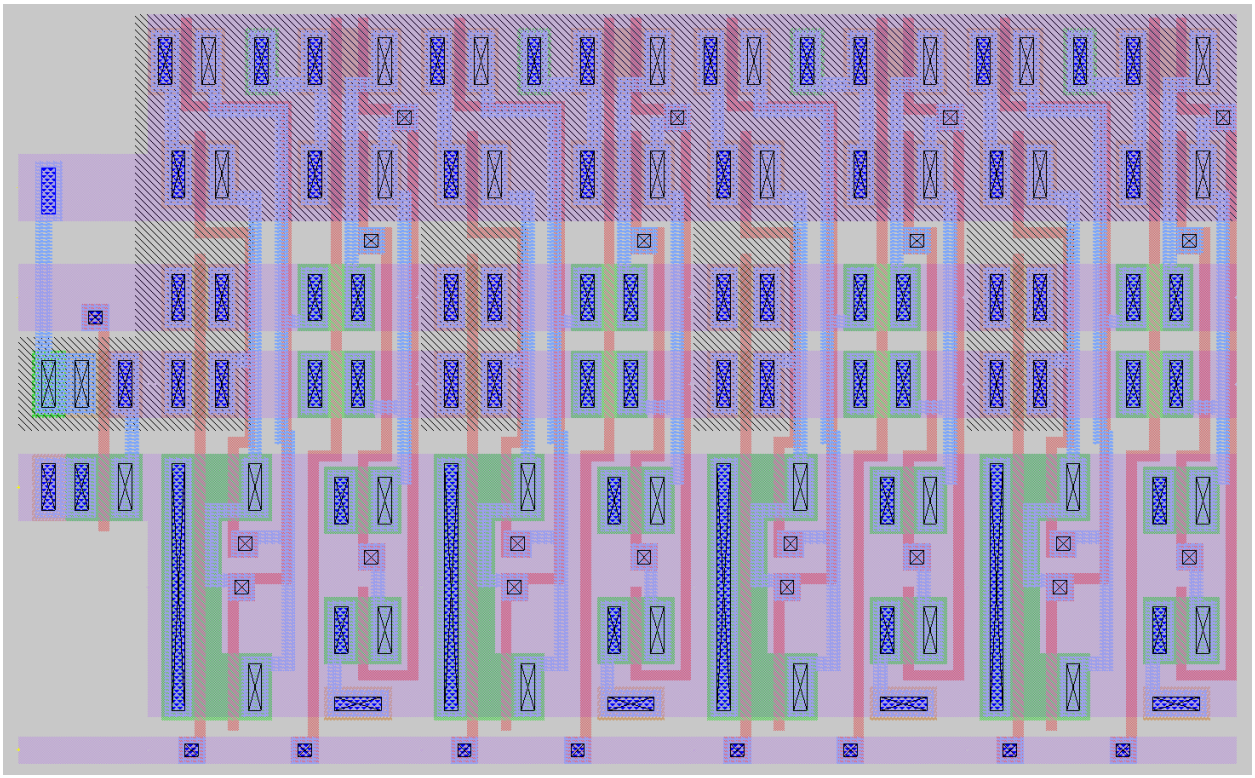

Figure 6: Four-bit shift register layout using Magic.

The dimensions of the entire register are 18.3μm by 11.25μm.

4 Layout Versus Schematic

The final step of the design is to create SPICE netlists for both the schematic and layout and use Netgen to check that the two netlists match. Running Netgen showed that the two netlists match uniquely.

```
Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 6 **Mismatch**             |Number of nets: 4 **Mismatch**
-----------------------------------------------------------------------------------------
NET mismatches: Class fragments follow (with fanout counts):
Circuit 1: inverter                        |Circuit 2: inverter
```

```
--------------------------------------------------------------------------------
Net: VP                                  |Net: VP
  sky130_fd_pr__pfet_01v8/(1|3) = 1      |  sky130_fd_pr__pfet_01v8/(1|3) = 1
                                         |  sky130_fd_pr__pfet_01v8/4 = 1
                                         |
Net: VN                                  |Net: VN
  sky130_fd_pr__nfet_01v8/(1|3) = 1      |  sky130_fd_pr__nfet_01v8/(1|3) = 1
                                         |  sky130_fd_pr__nfet_01v8/4 = 1
                                         |
Net: GND                                 |(no matching net)
  sky130_fd_pr__nfet_01v8/4 = 1          |
                                         |
Net: VDD                                 |(no matching net)
  sky130_fd_pr__pfet_01v8/4 = 1          |
--------------------------------------------------------------------------------
Netlists do not match.
  Flattening non-matched subcircuits inverter inverter

Subcircuit summary:
Circuit 1: csrl_flipflop                 |Circuit 2: csrl_flipflop
-----------------------------------------|-----------------------------------------
sky130_fd_pr__nfet_01v8 (7)              |sky130_fd_pr__nfet_01v8 (7)
sky130_fd_pr__pfet_01v8 (8)              |sky130_fd_pr__pfet_01v8 (8)
Number of devices: 15                    |Number of devices: 15
Number of nets: 14 **Mismatch**          |Number of nets: 12 **Mismatch**
--------------------------------------------------------------------------------
NET mismatches: Class fragments follow (with fanout counts):
Circuit 1: csrl_flipflop                 |Circuit 2: csrl_flipflop

--------------------------------------------------------------------------------
Net: VN                                  |Net: VN
  sky130_fd_pr__nfet_01v8/(1|3) = 3      |  sky130_fd_pr__nfet_01v8/(1|3) = 3
                                         |  sky130_fd_pr__nfet_01v8/4 = 7
                                         |
Net: VP                                  |Net: VP
  sky130_fd_pr__pfet_01v8/(1|3) = 4      |  sky130_fd_pr__pfet_01v8/(1|3) = 4
                                         |  sky130_fd_pr__pfet_01v8/4 = 8
                                         |
Net: VDD                                 |(no matching net)
  sky130_fd_pr__pfet_01v8/4 = 8          |
                                         |
Net: GND                                 |(no matching net)
  sky130_fd_pr__nfet_01v8/4 = 7          |
--------------------------------------------------------------------------------
Netlists do not match.
  Flattening non-matched subcircuits csrl_flipflop csrl_flipflop

Subcircuit summary:
Circuit 1: four_bit_shift_register_xschem. |Circuit 2: four_bit_shift_register.spice
-------------------------------------------|-----------------------------------------
sky130_fd_pr__nfet_01v8 (29)               |sky130_fd_pr__nfet_01v8 (29)
sky130_fd_pr__pfet_01v8 (33)               |sky130_fd_pr__pfet_01v8 (33)
Number of devices: 62                      |Number of devices: 62
Number of nets: 33                         |Number of nets: 33
```

```
--------------------------------------------------------------------------------
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes four_bit_shift_register_xschem.spice and four_bit_shift_register.spice are equivalent.

Final result: Circuits match uniquely.
.
```