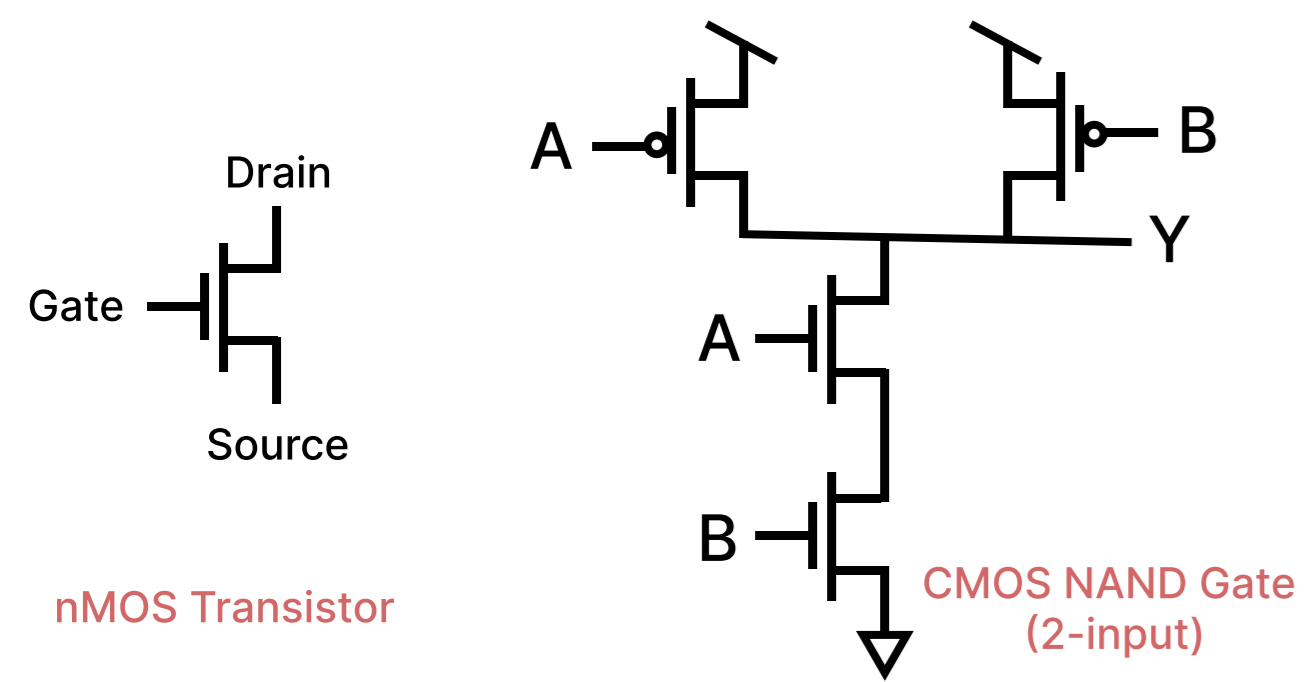


Euler Paths for Optimization of CMOS Integrated Circuit Layouts

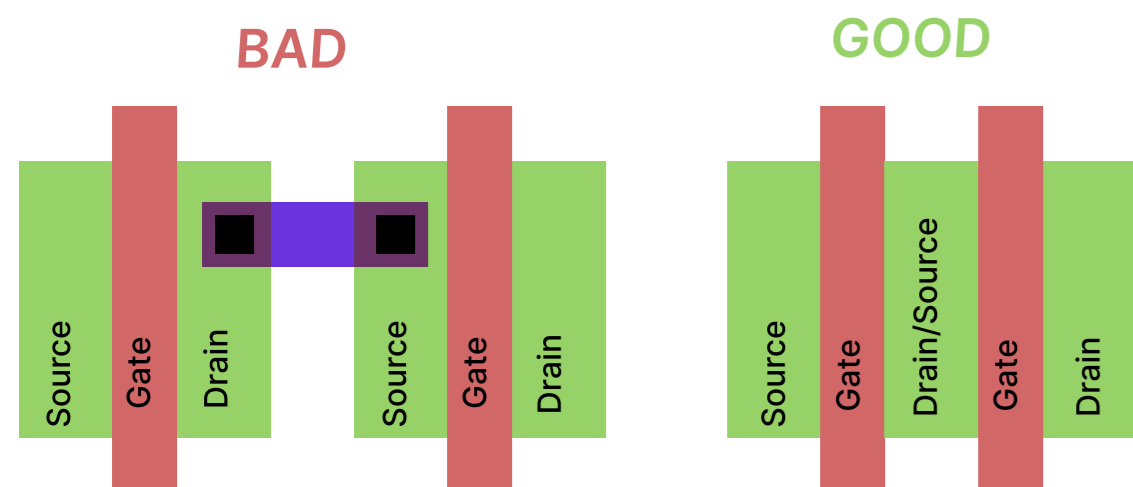
Marc Eftimie, Luke Witten, Kenta Burpee

Transistors and Logic Gates

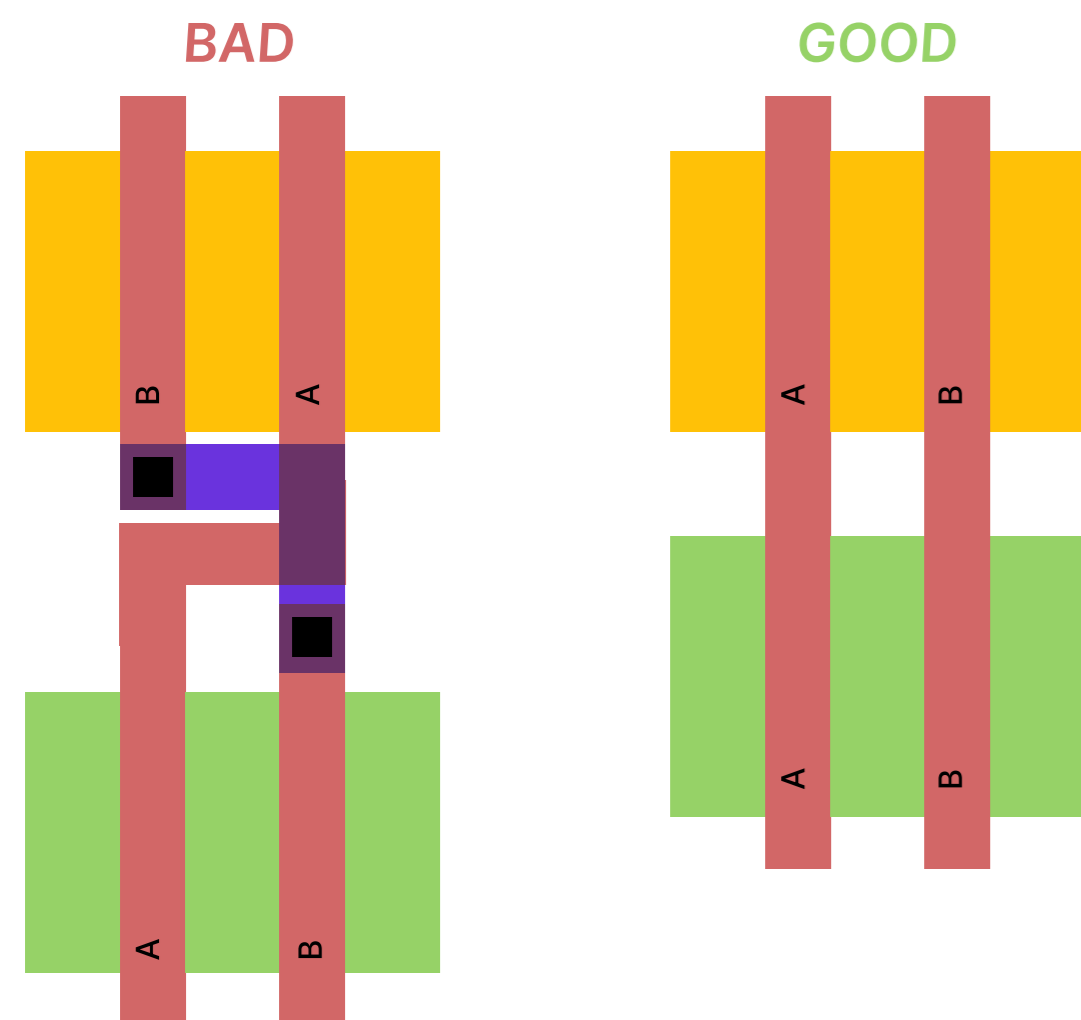


Integrated Circuit Layout Design

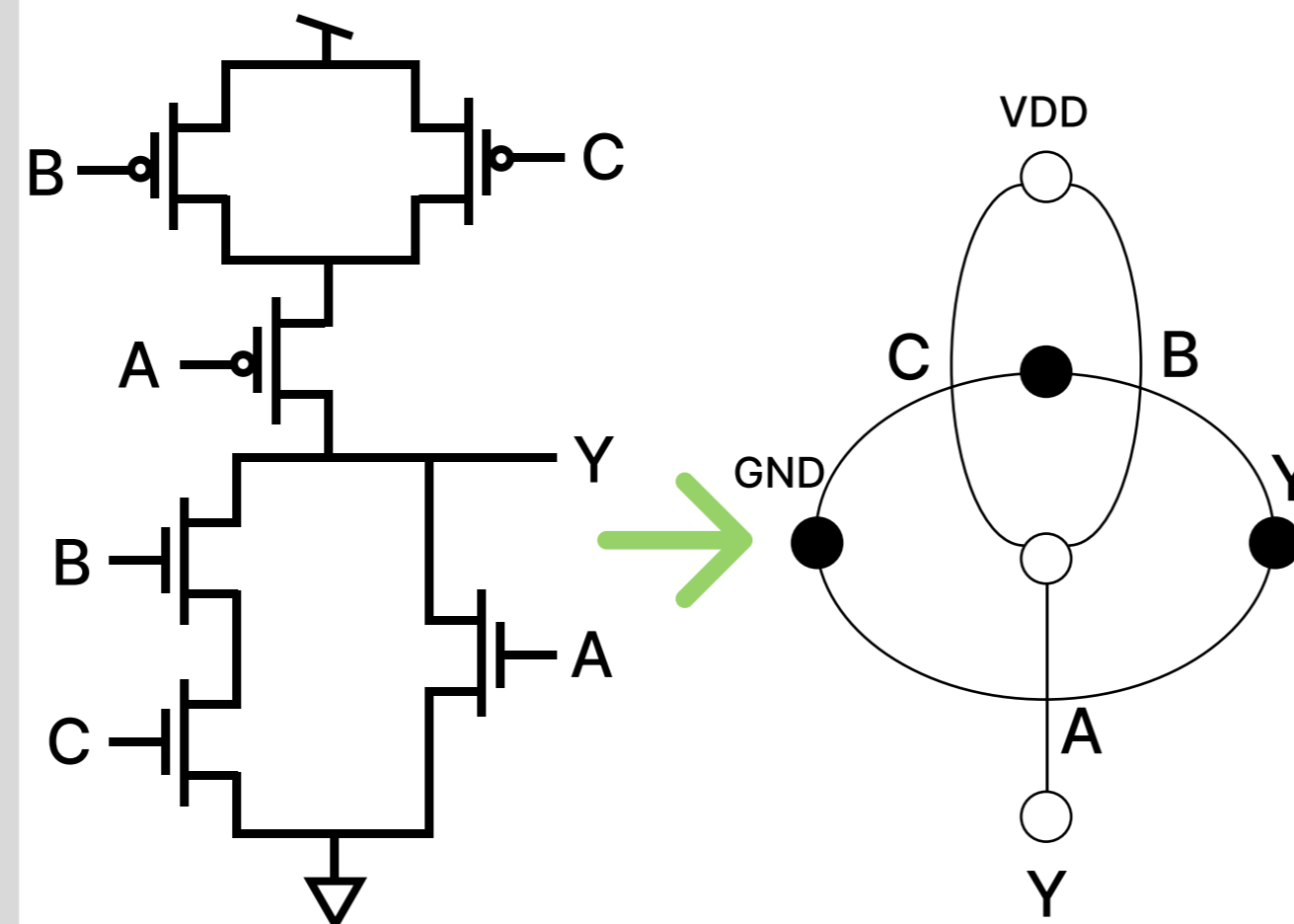
Connecting Source/Drain Regions



Connecting Gates



Converting Schematics to Graphs

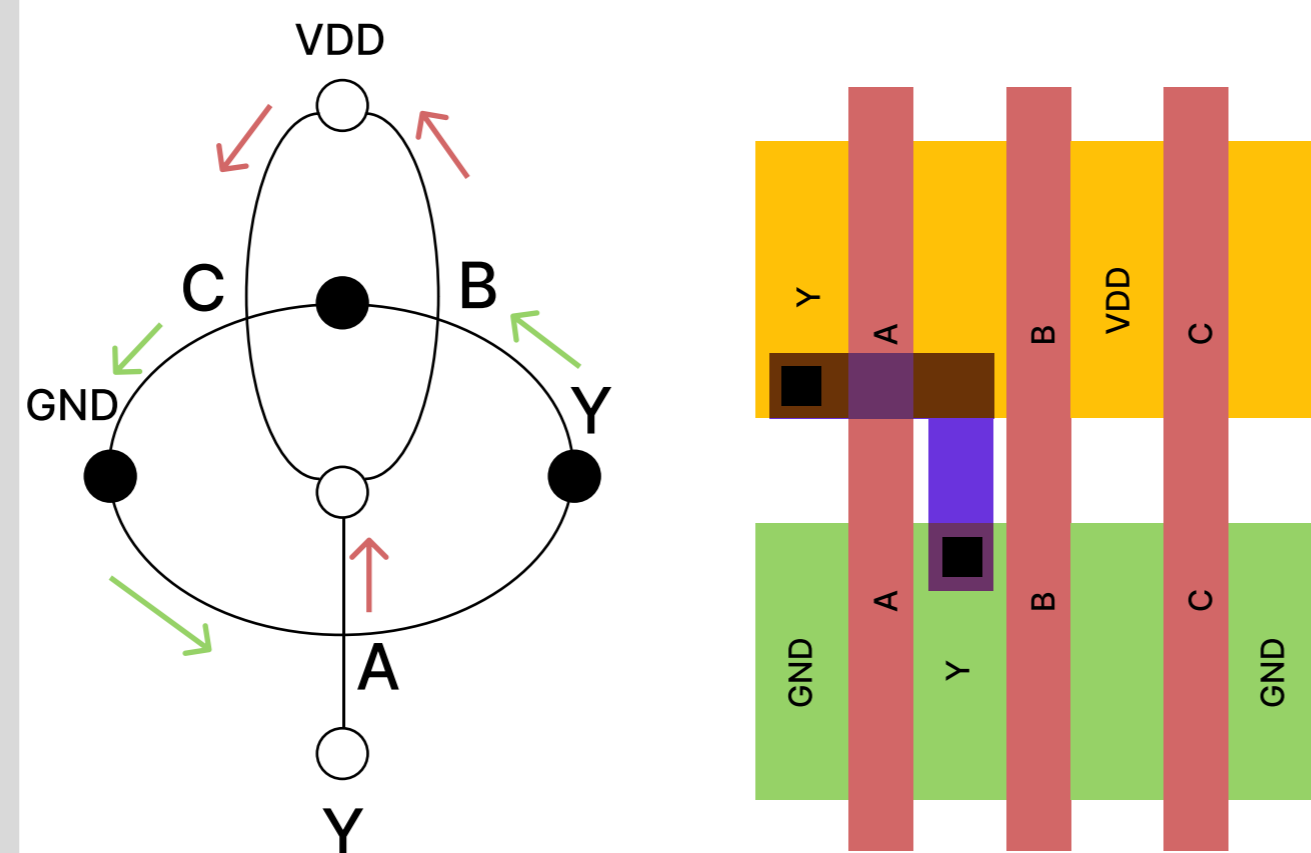


$$Y = \sim A * (\sim B + \sim C)$$

- Vertices: nodes
- Edges: transistors

Euler Paths

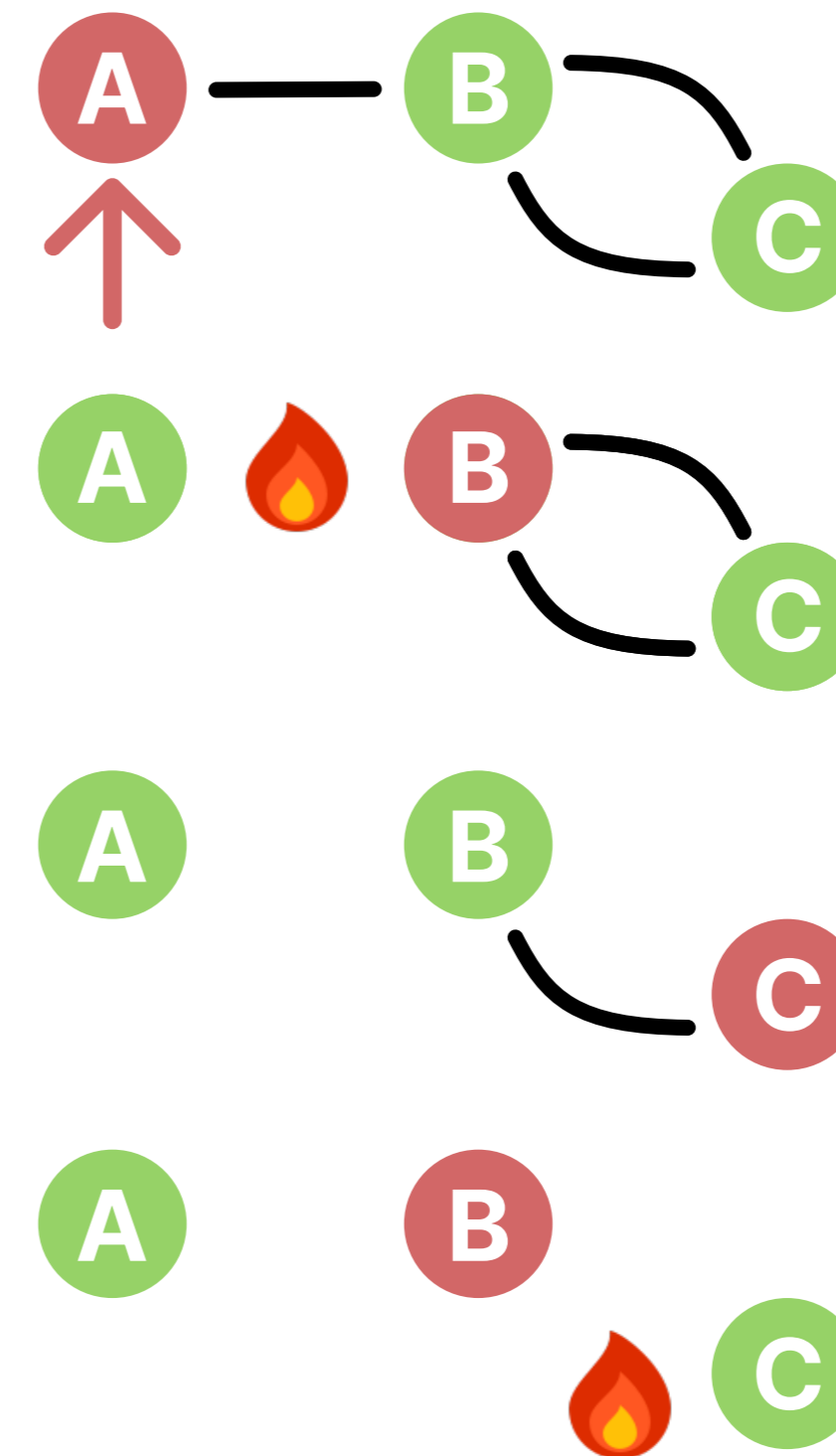
- Euler paths traverse all edges in a graph once
- Euler paths maximize source/drain region sharing
- Matching Euler paths avoid polysilicon (gate) crossings



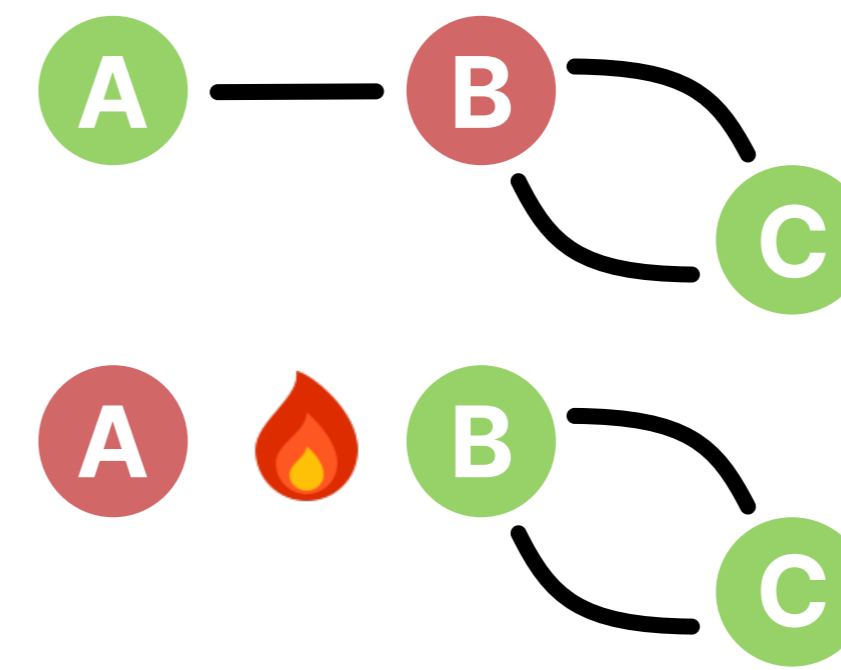
A → B → C: Matching Euler Paths

Fleury's Algorithm

Walk n' Burn



Don't Burn Bridges! (unless necessary)

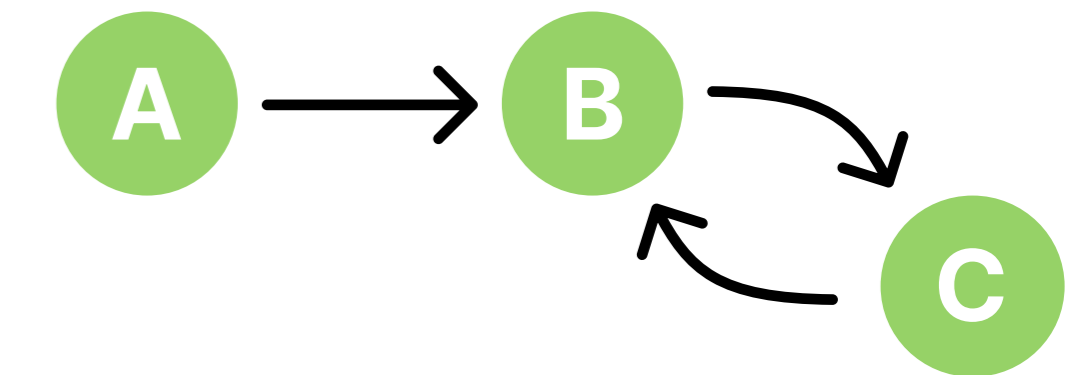


Stuck on A!

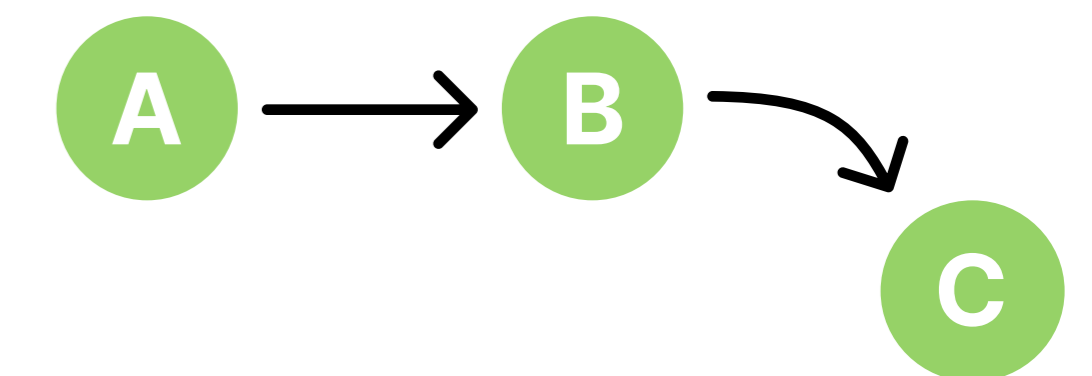
Our Modifications

Our script finds ALL Euler Paths in a graph using **backtracking**

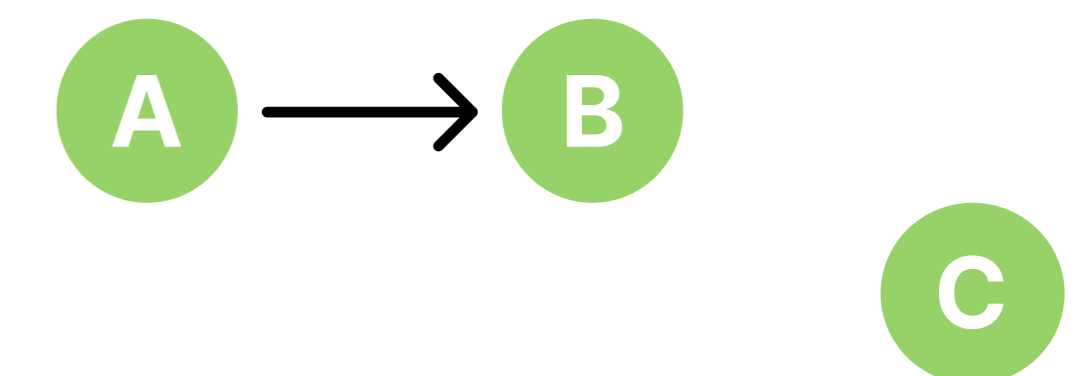
Find Euler path using **Fleury's Algorithm**



Backtrack to C to explore new paths



No new nodes to go to from C, **backtrack** to B



Explore new path from B to C using **Fleury's Algorithm**

